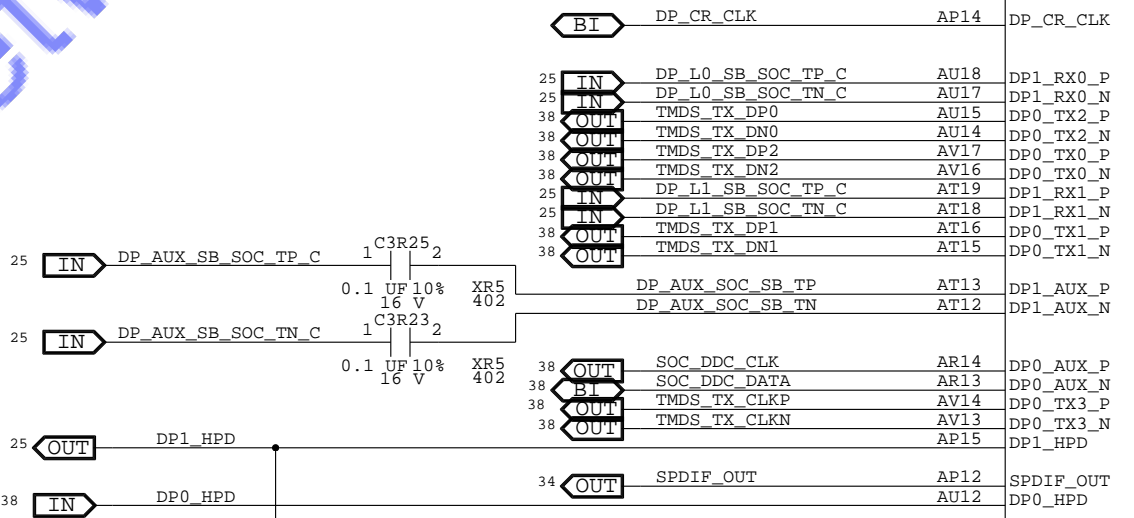
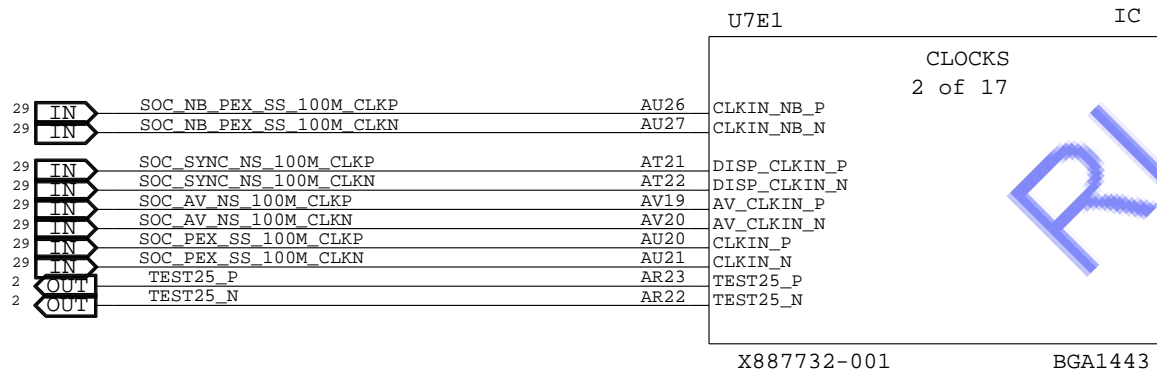
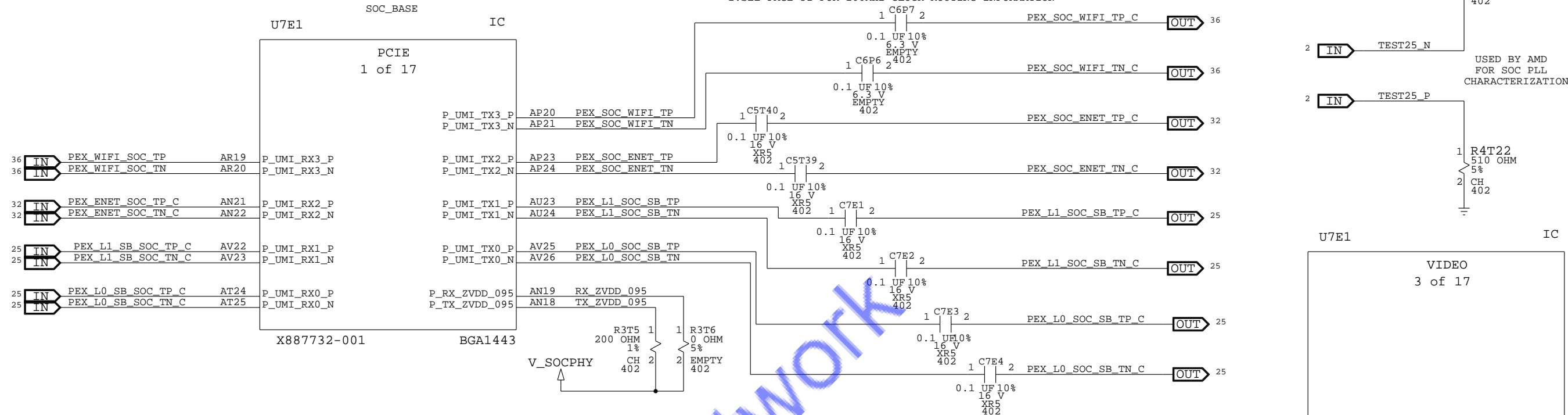


8		7		6		5		4		3		2		1		
D	PAGE	CONTENTS													D	
	[1]	COVER PAGE														
	[2]	SOC: PCIEX,CLOCKS,VIDEO														
	[3]	SOC: POWER: MEMIO,CPUCORE,NBCORE,MISC														
	[4]	SOC: POWER: V_GFXCORE,VSS														
	[5]	SOC: MEMORY PARTITION C & D														
	[6]	SOC: MEMORY PARTITION A & B														
	[7]	SOC: VSS, SPARE														
	[8]	SOC: DEBUG, SB SIGNALS														
	[9]	SOC: DECOUPLING														
C	[10]	SOC: DECOUPLING													C	
	[11]	SOC: DECOUPLING														
	[12]	MEMORY: CHANNEL D														
	[13]	MEMORY: CHANNEL D														
	[14]	MEMORY: CHANNEL D, DECOUPLING & TERMINATION														
	[15]	MEMORY: CHANNEL C														
	[16]	MEMORY: CHANNEL C														
	[17]	MEMORY: CHANNEL C, DECOUPLING & TERMINATION														
	[18]	MEMORY: CHANNEL B														
	[19]	MEMORY: CHANNEL B														
B	[20]	MEMORY: CHANNEL B, DECOUPLING & TERMINATION													B	
	[21]	MEMORY: CHANNEL A														
	[22]	MEMORY: CHANNEL A														
	[23]	MEMORY: CHANNEL A, DECOUPLING & TERMINATION														
	[24]	KIC: USB														
	[25]	KIC: PCIEX, SATA, VIDEO														
	[26]	KIC: SMC														
	[27]	KIC: FACET														
	[28]	KIC: POWER														
	[29]	KIC: CLOCKS, STRAPPING, POR														
A	[30]	KIC: POWER													A	
	[31]	KIC: DECOUPLING														
	[32]	ETHERNET CONTROLLER														
	[33]	EMMC														
	[34]	CONN: RJ45,TOSLINK														
	[35]	CONN: USB (FRONT & REAR)														
	[36]	CONN: WIFI														
	[37]	CONN: HDMI IN														
	[38]	CONN: HDMI OUT														
	[39]	CONN: HDMI SUPPORT														
[40]	CONN: ODD & HDD															
[41]	CONN: FRONT PANEL, FAN, AUDIO															
[42]	CONN: POWER															
[43]	VREGS: INPUT & OUTPUT FILTERS															
[44]	VREGS: CPUCORE															
[45]	VREGS: GFXCORE															
[46]	VREGS: GFXCORE OUTPUT PHASE 1 & 2															
[47]	VREGS: CPUCORE OUTPUT PHASE															
8		7		6		5		4		3		2		1		

# SOC:PCIEX,CLOCKS,VIDEO

## NOTES:

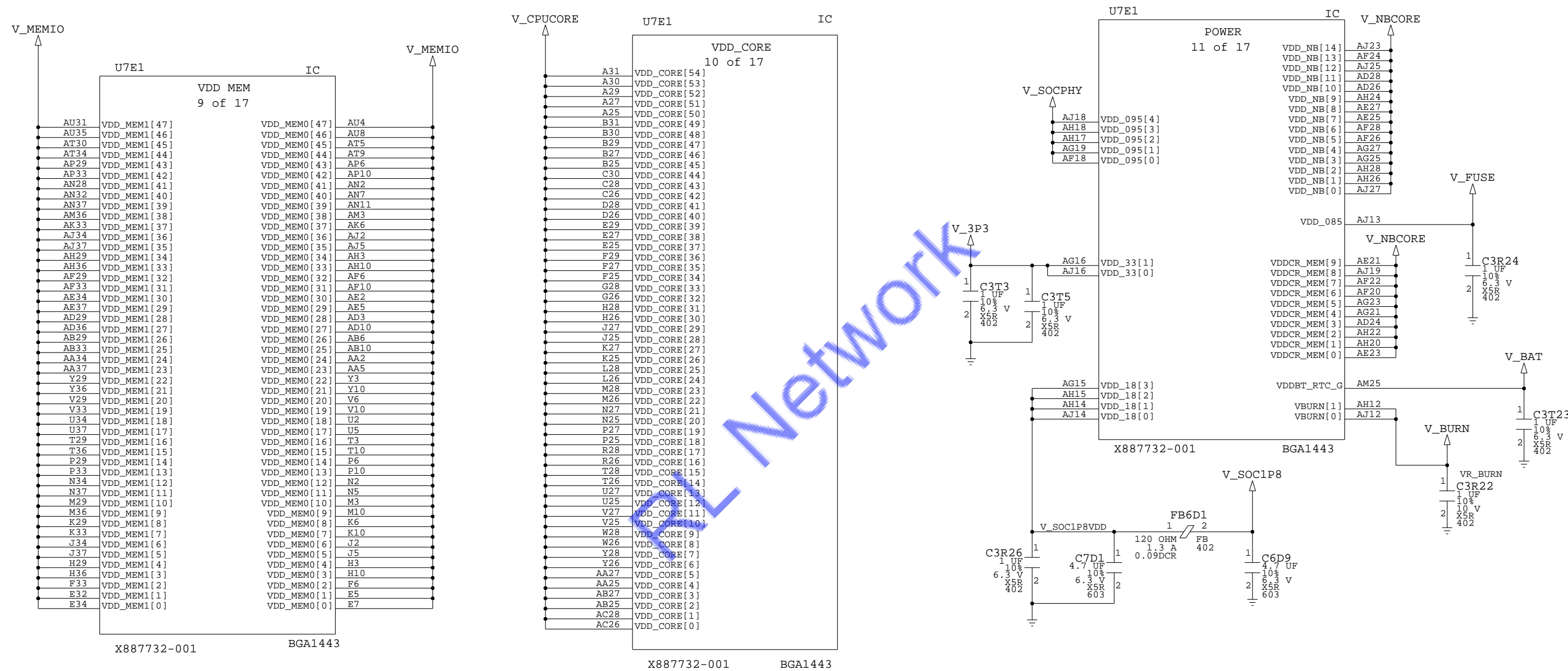
- 1.TO SUPPORT A PCIE WIFI INTERFACE (J3C1), POPULATE C6P6 AND C6P7
- 2.SEE PAGE 32 FOR 100MHZ CLOCK ROUTING INFORMATION

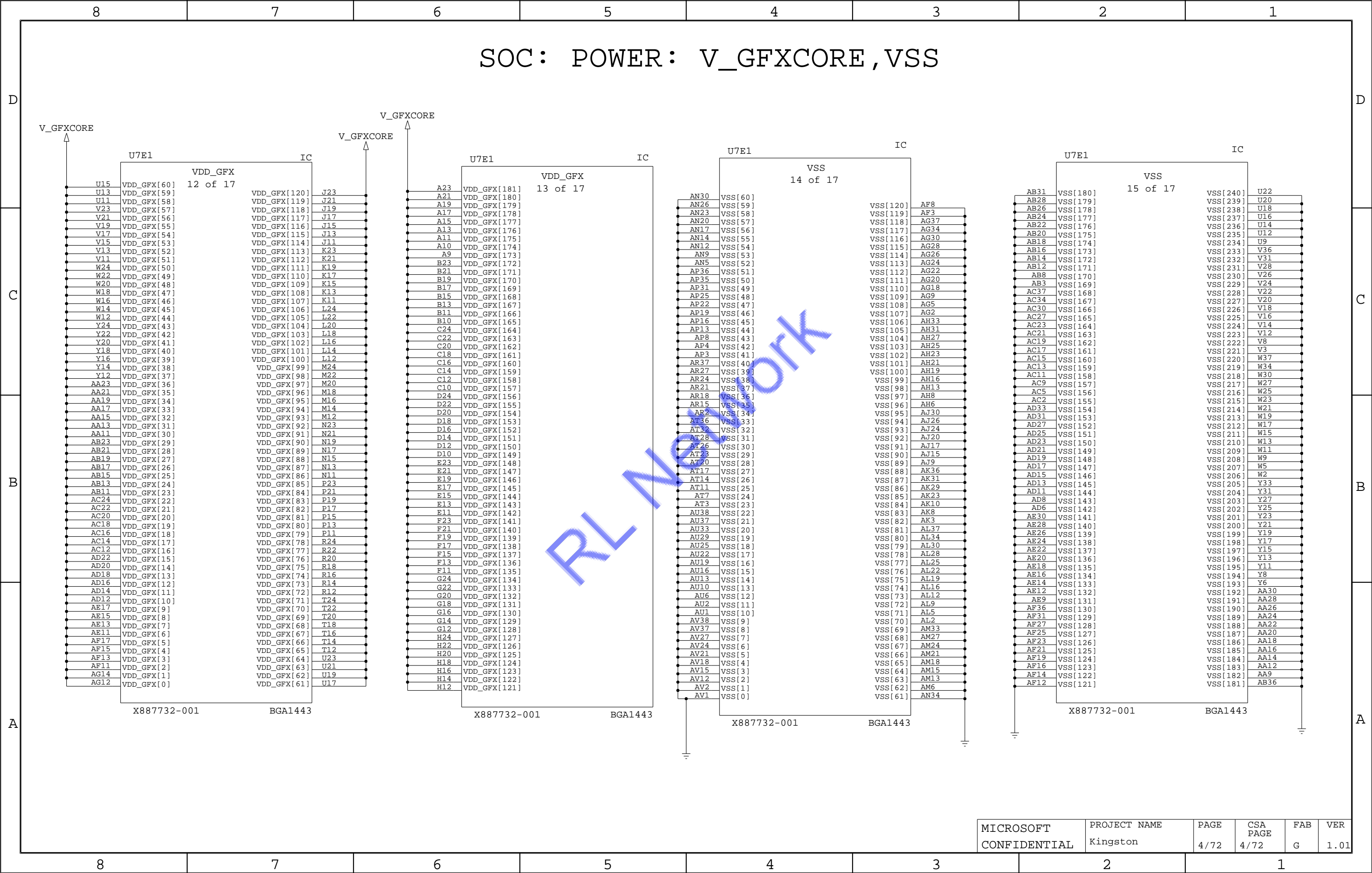


DVI PCB ROUTING ORDERING	DP PCB ROUTING ORDERING	PIN NAME
TMDS CLOCK -	DP LANE 3 -	DP0_TX3_N
TMDS CLOCK +	DP LANE 3 +	DP0_TX3_P
TMDS DATA0 -	DP LANE 2 -	DP0_TX2_N
TMDS DATA0 +	DP LANE 2 +	DP0_TX2_P
TMDS DATA1 -	DP LANE 1 -	DP0_TX1_N
TMDS DATA1 +	DP LANE 1 +	DP0_TX1_P
TMDS DATA2 -	DP LANE 0 -	DP0_TX0_N
TMDS DATA2 +	DP LANE 0 +	DP0_TX0_P

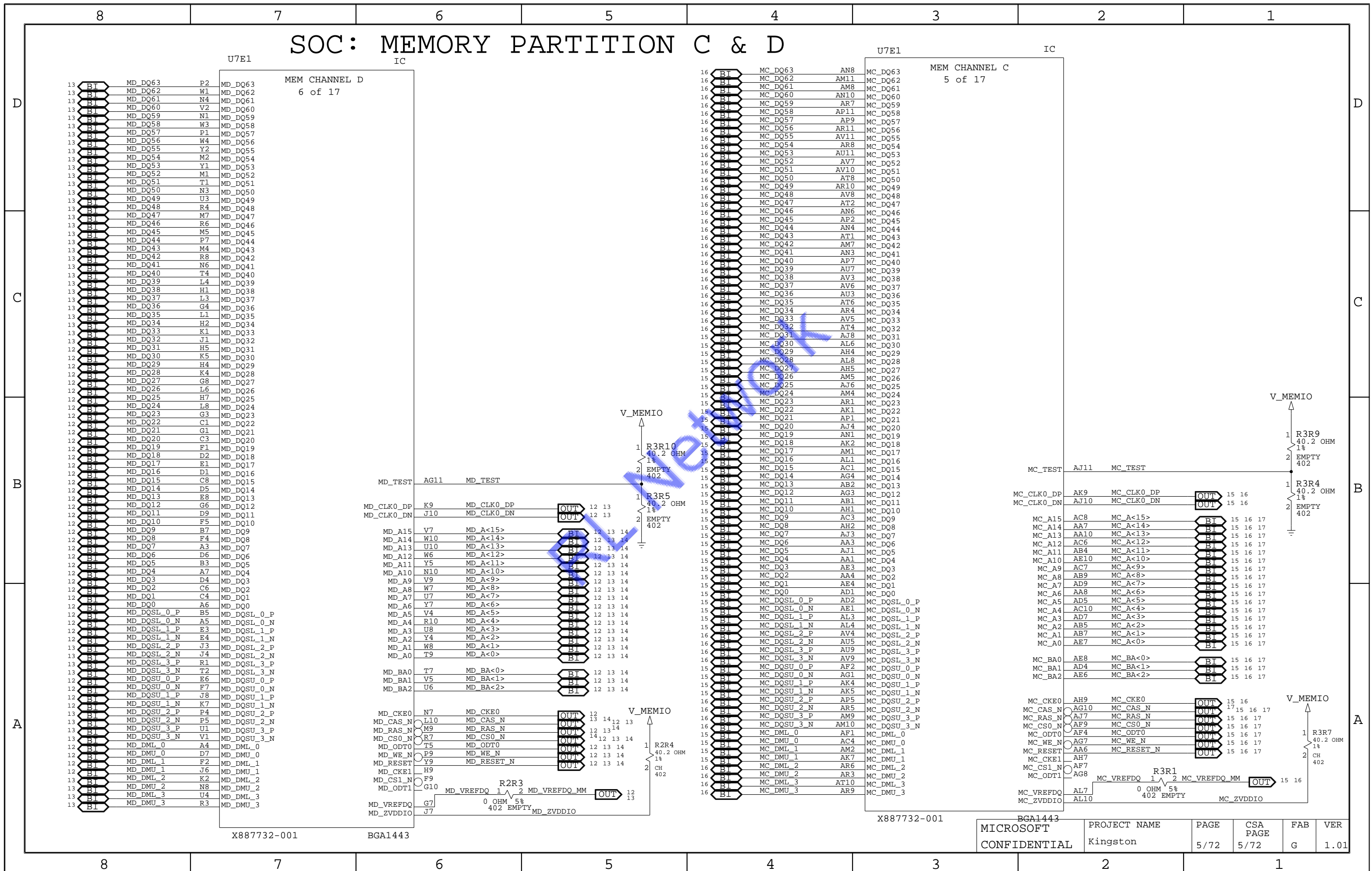
MS_PART#	MATL	REF DES	DESCR.	BOM PROPERTY
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X941294-001	IC	U7E1	ARLENE,TSMC,IRIDEN,SPIL,AMD PENANG,TYPICAL,79W TDP+,AG,AKA ROUTE	ARLENE_SOC_R2
X941295-001	IC	U7E1	ARLENE,TSMC,UMTC,SPIL,AMD PENANG,TYPICAL,79W TDP+,AG,AKA ROUTE	ARLENE_SOC_R3
X941296-001	IC	U7E1	ARLENE,TSMC,NOT DEFINED,SPIL,AMD PENANG,FF,79W TDP+,AG	ARLENE_SOC_FF
X941297-001	IC	U7E1	ARLENE,TSMC,NOT DEFINED,SPIL,AMD PENANG,FS,79W TDP+,AG	ARLENE_SOC_FS
X941298-001	IC	U7E1	ARLENE,TSMC,NOT DEFINED,SPIL,AMD PENANG,SF,79W TDP+,AG	ARLENE_SOC_SF
X941299-001	IC	U7E1	ARLENE,TSMC,NOT DEFINED,SPIL,AMD PENANG,SS,79W TDP+,AG	ARLENE_SOC_SS

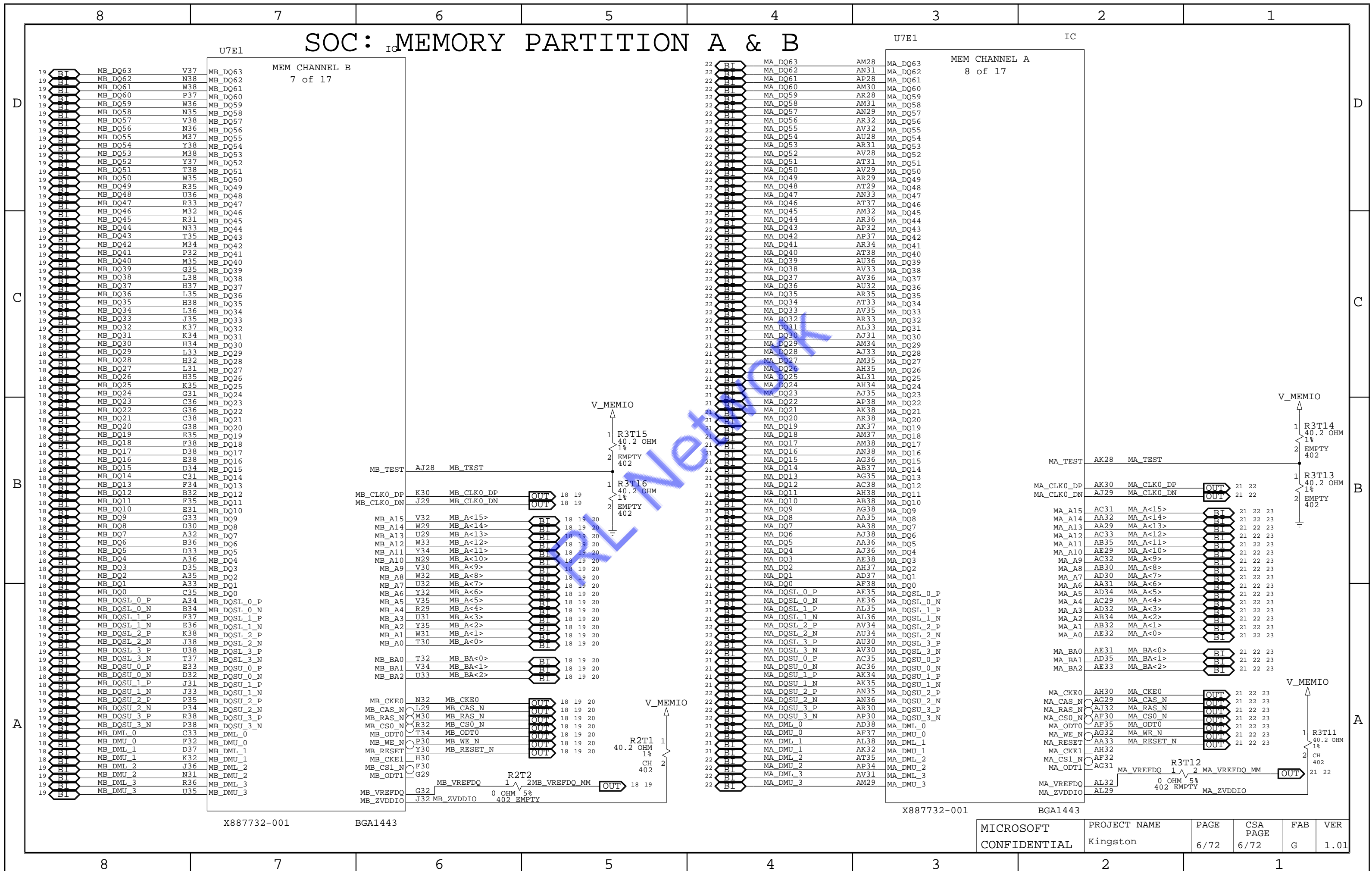
SOC: POWER: MEMIO, MEMCORE, CPUCORE, NBCORE, MISC

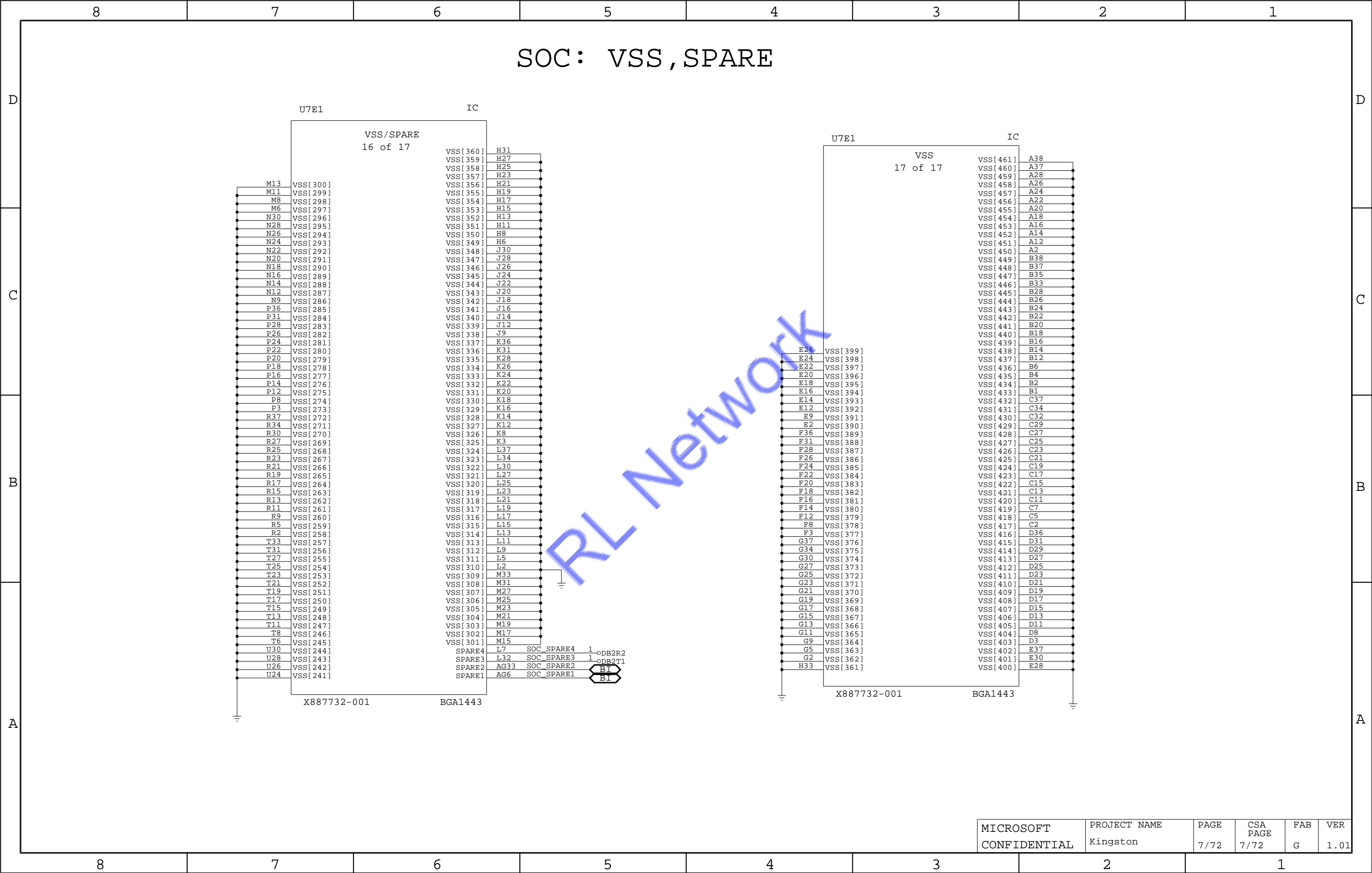




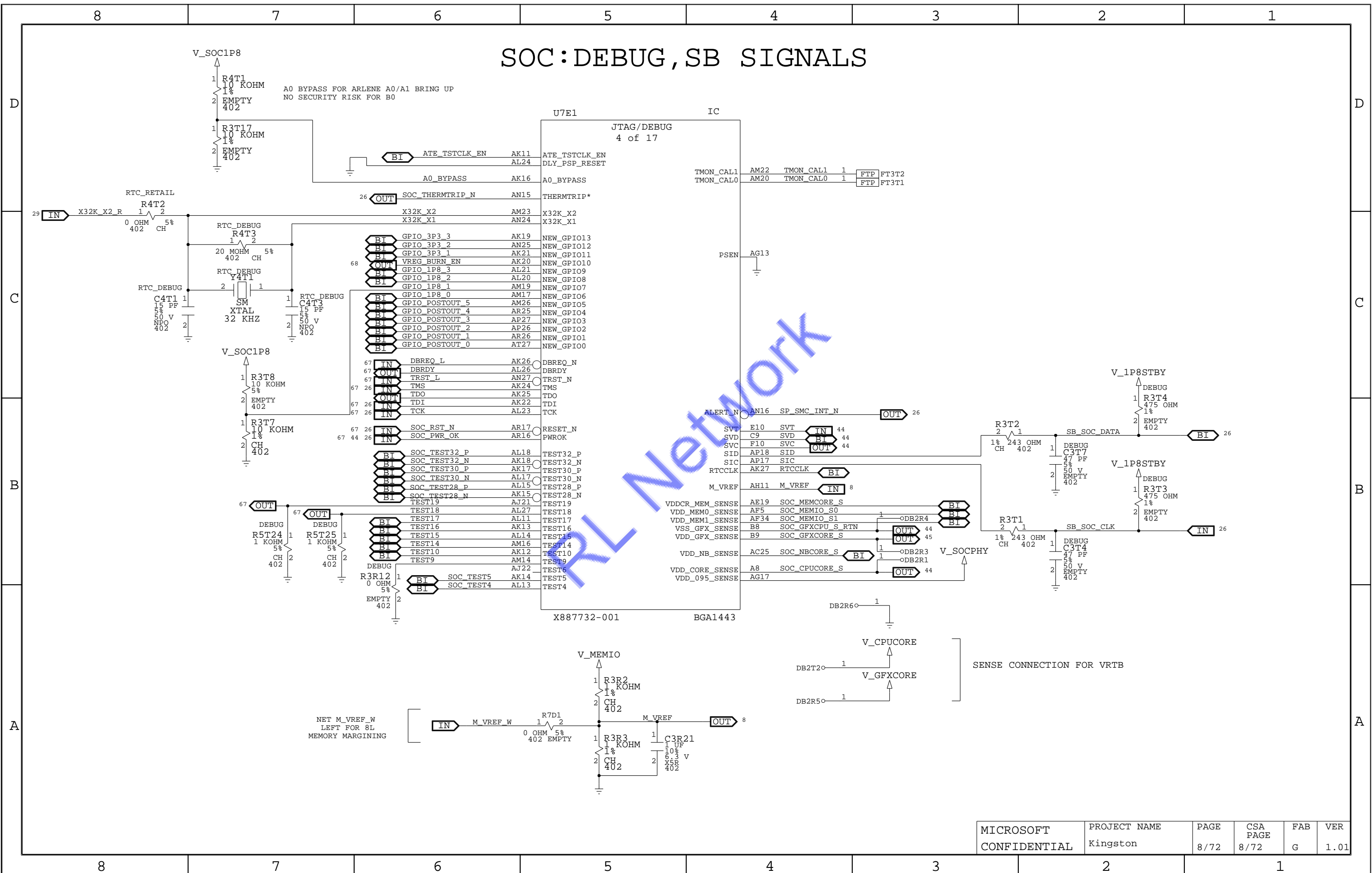










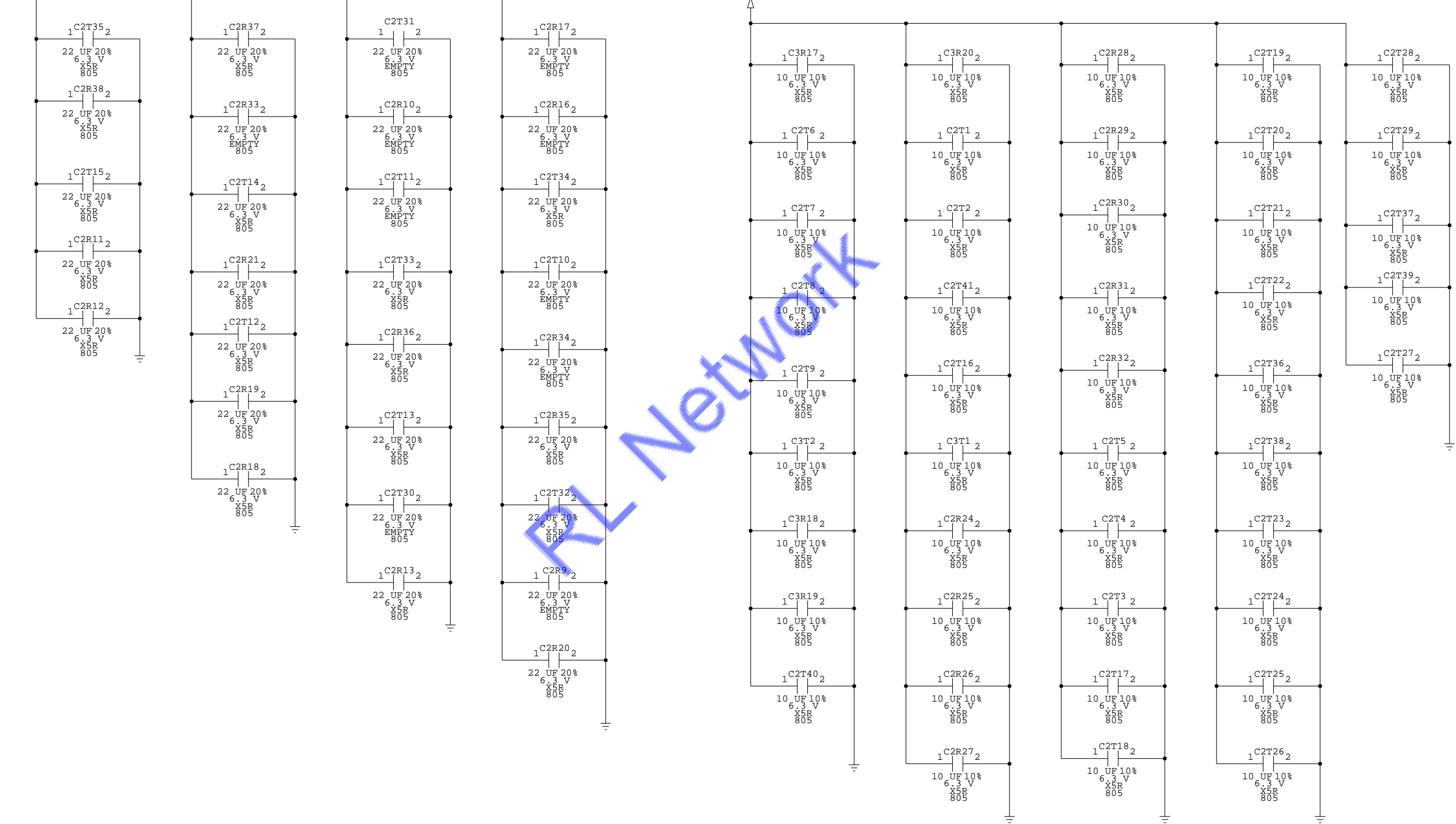


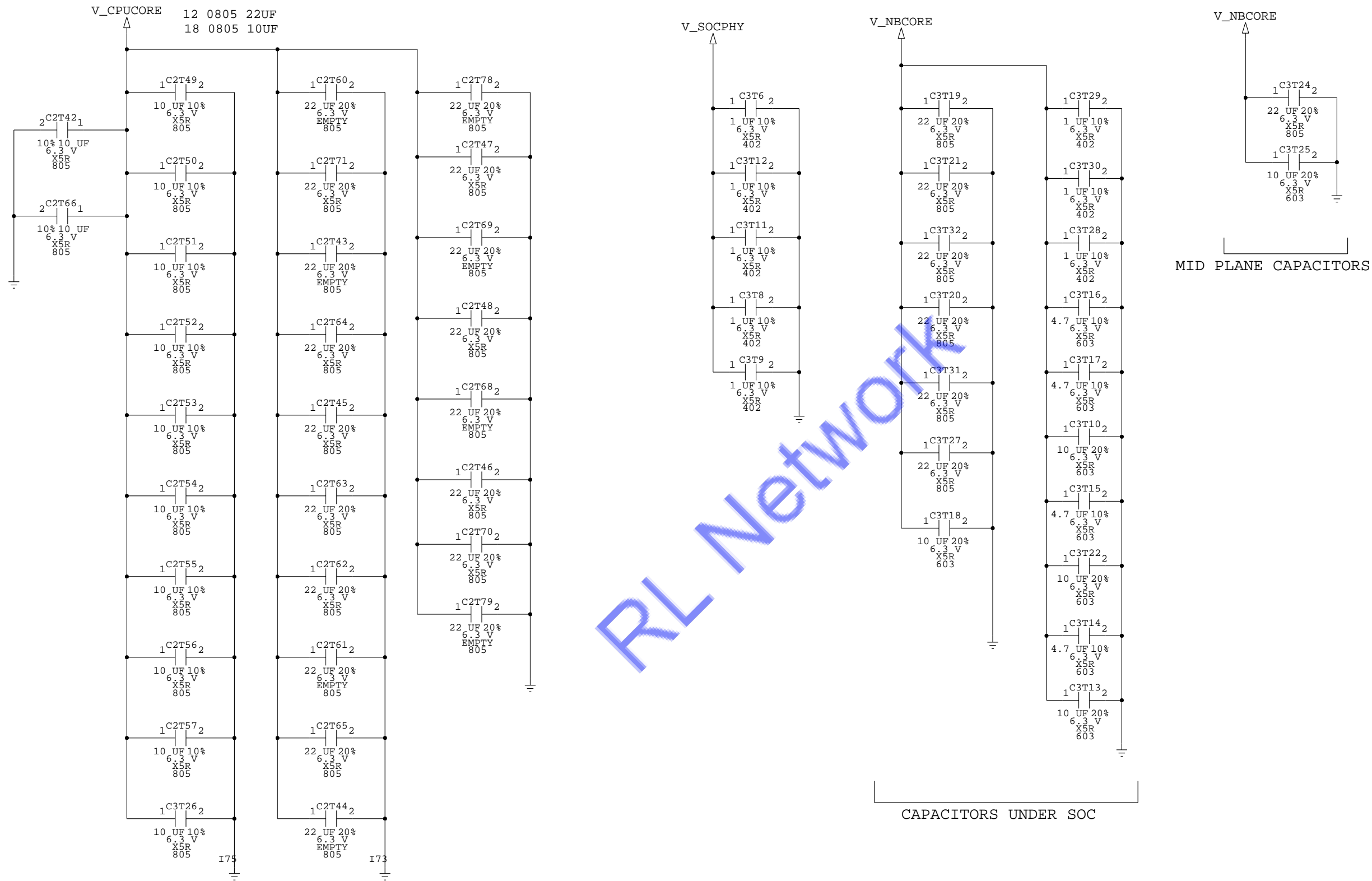


SOC: DECOUPLING

V\_GFXCORE 29 0805 22UF

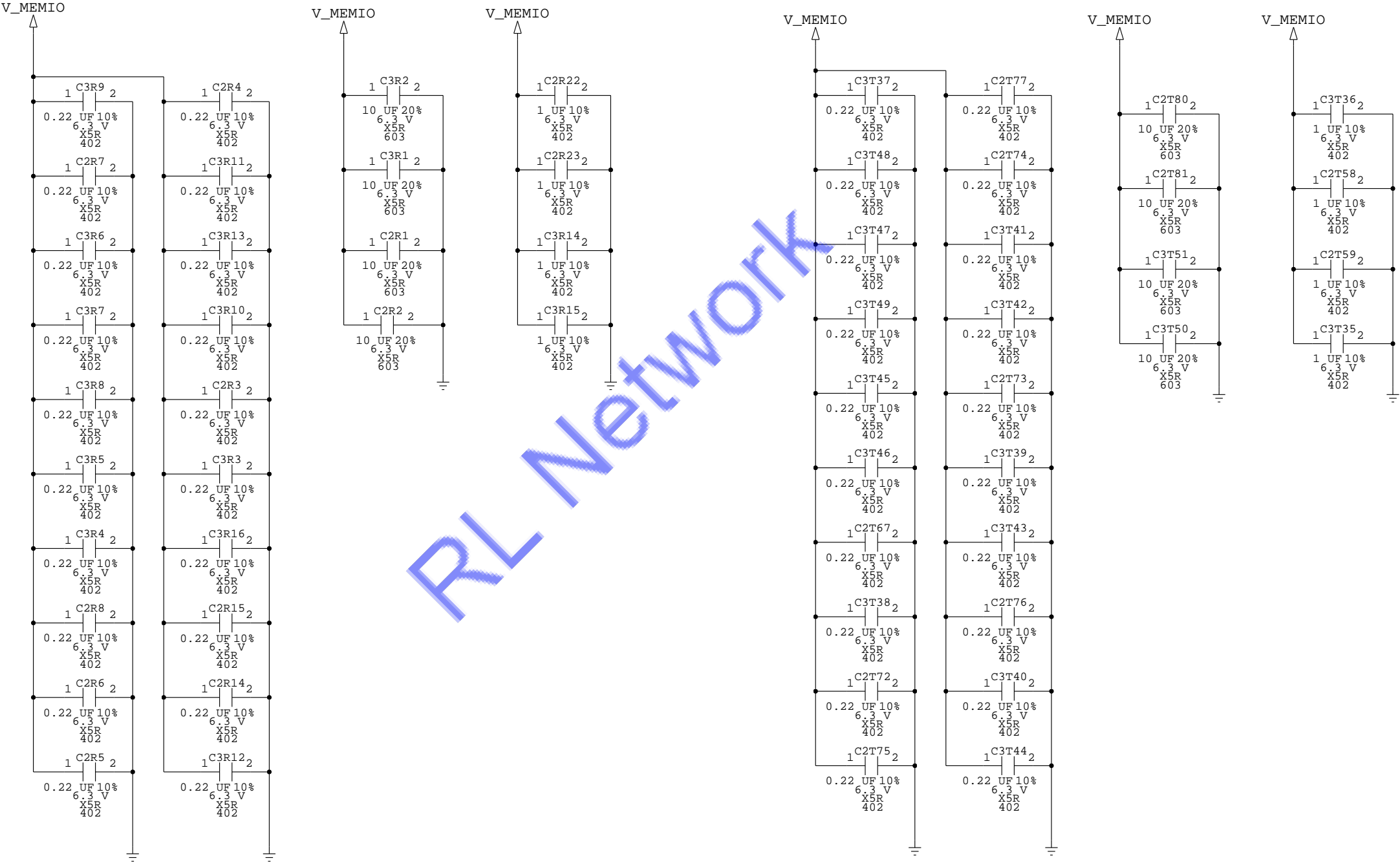
V\_GFXCORE 44 0805 10UF





MICROSOFT CONFIDENTIAL	PROJECT NAME Kingston	PAGE 10/72	CSA PAGE 10/72	FAB G	VER 1.01
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# SOC: DECOUPLING



MEMORY: CHANNEL D

D

C

B

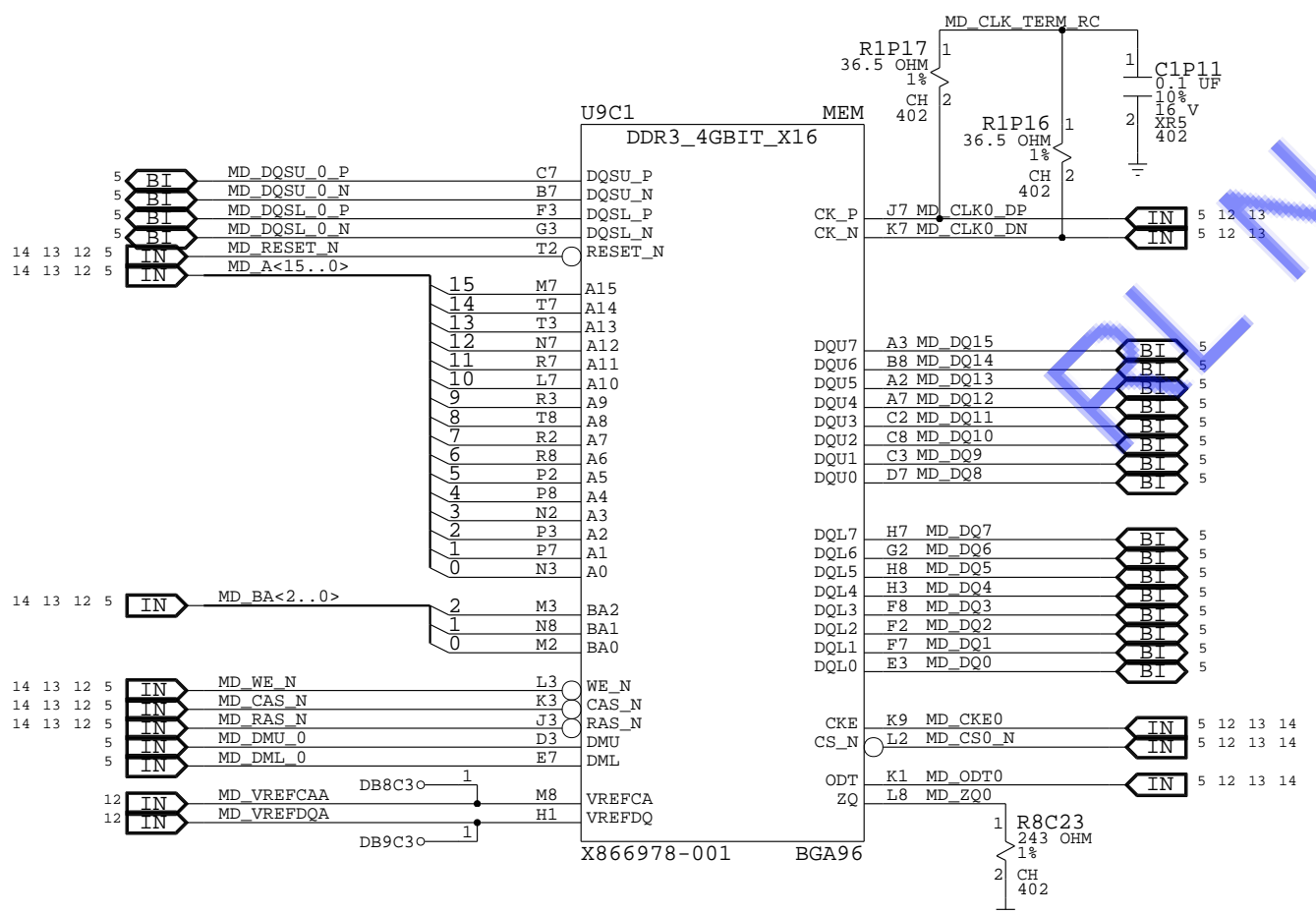
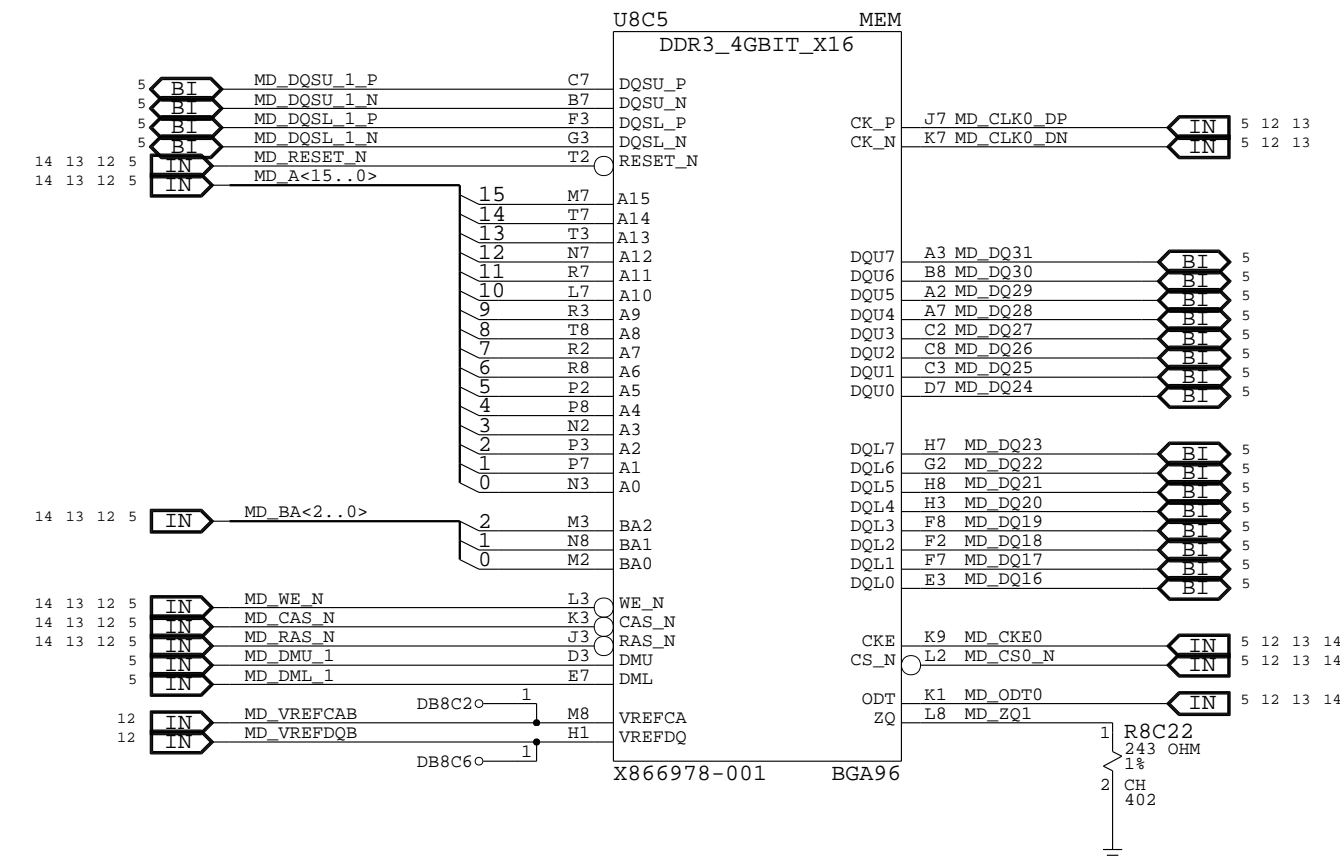
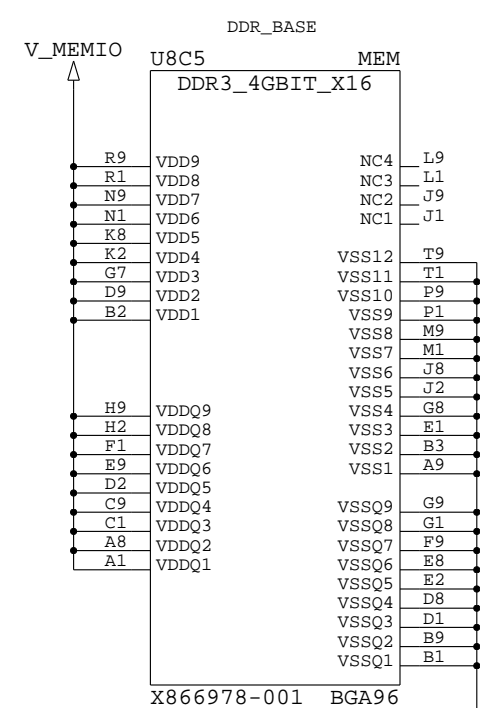
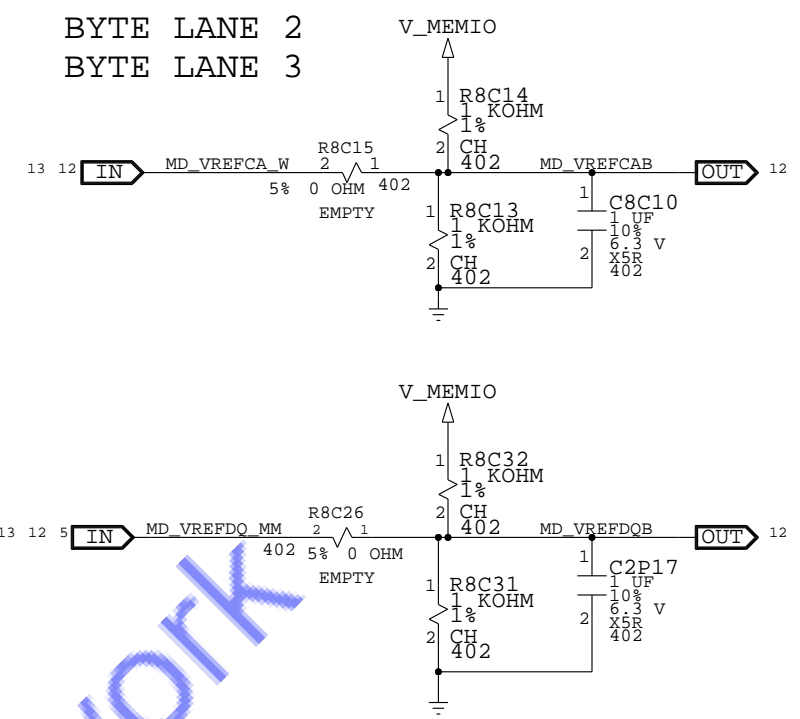
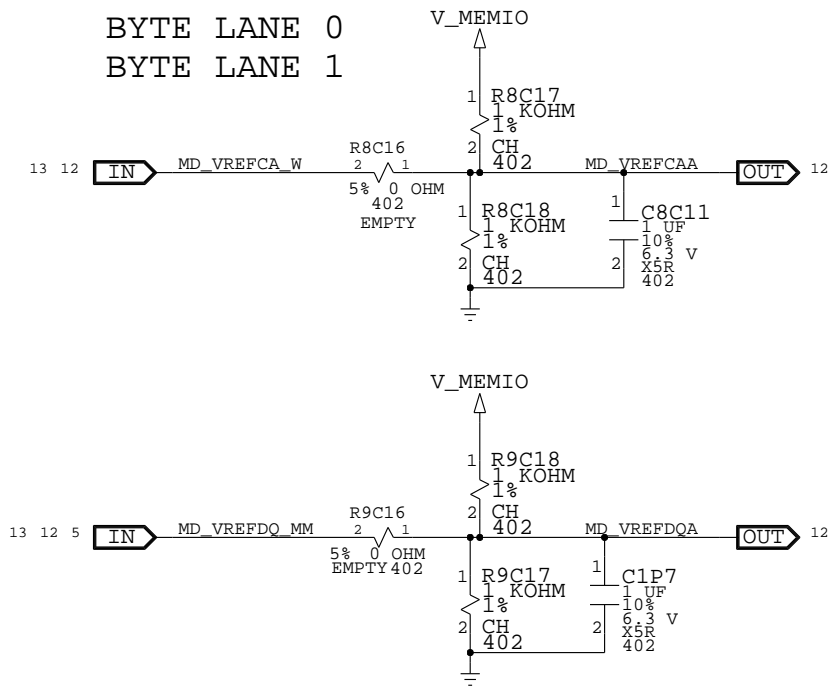
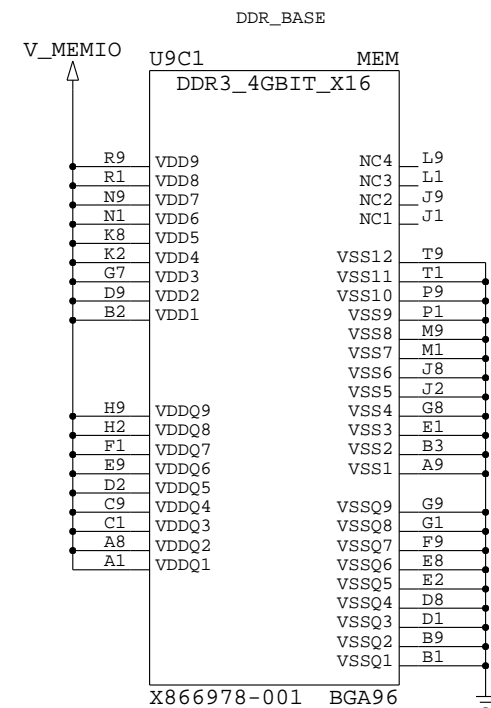
A

D

C

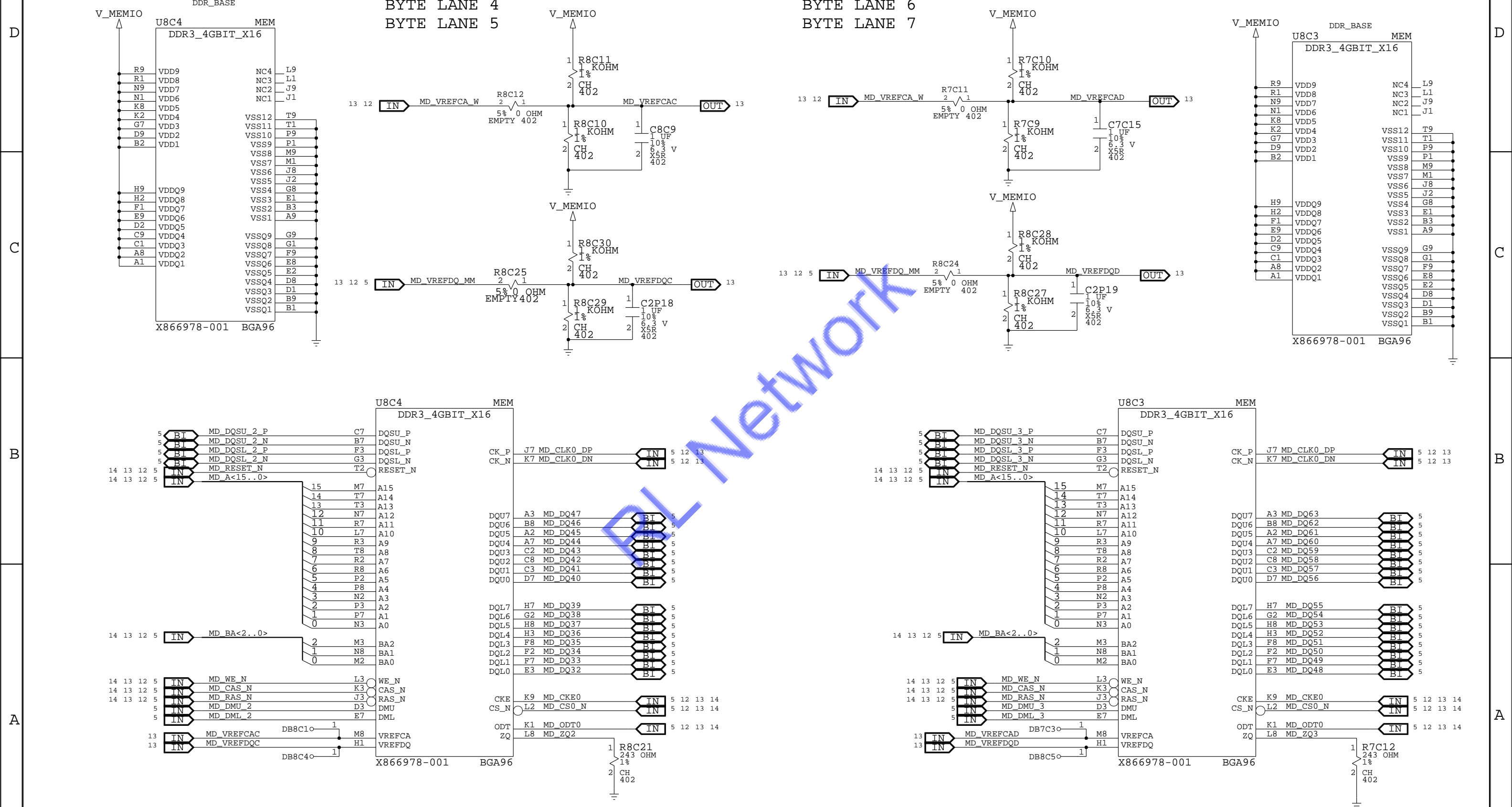
B

A

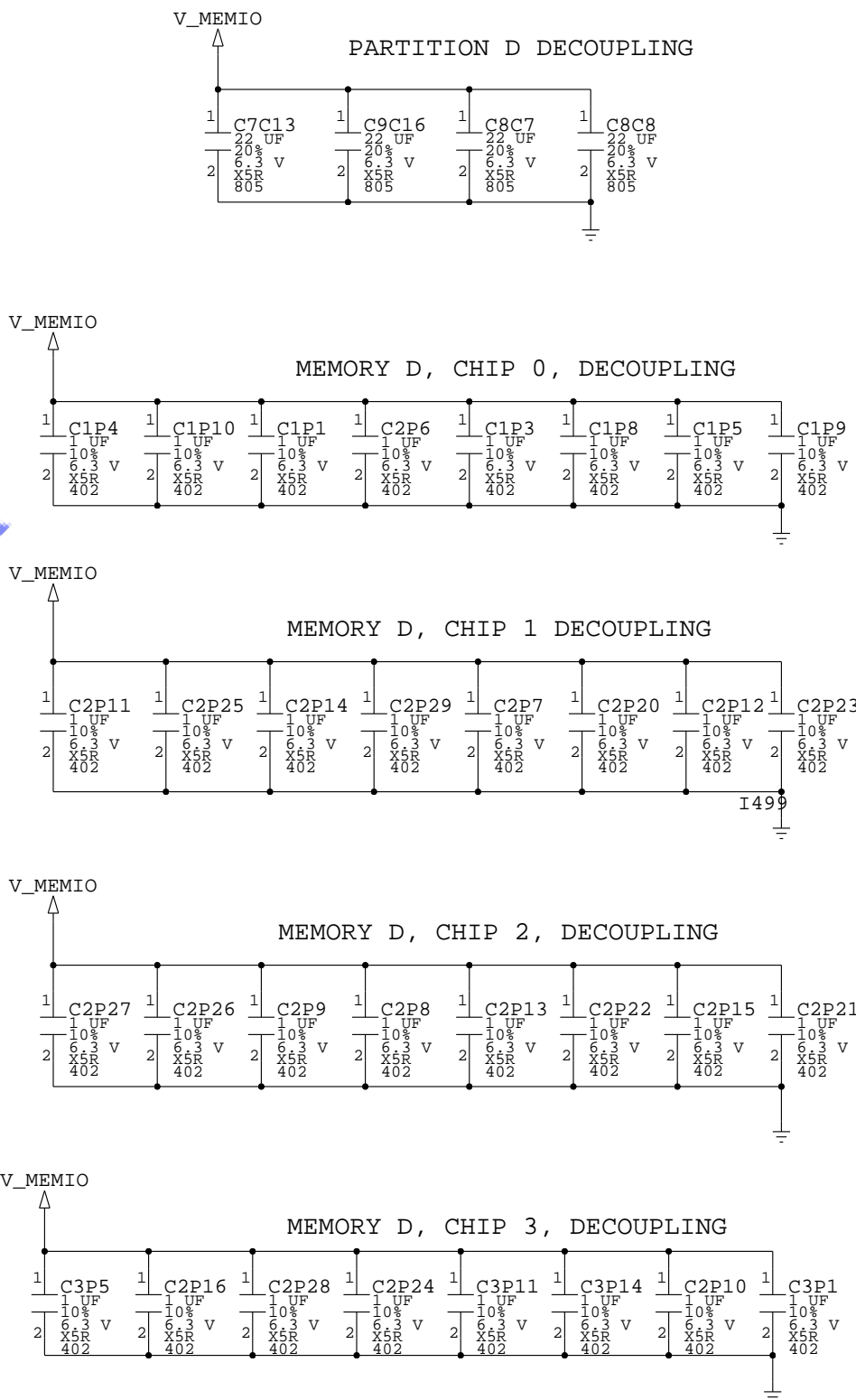
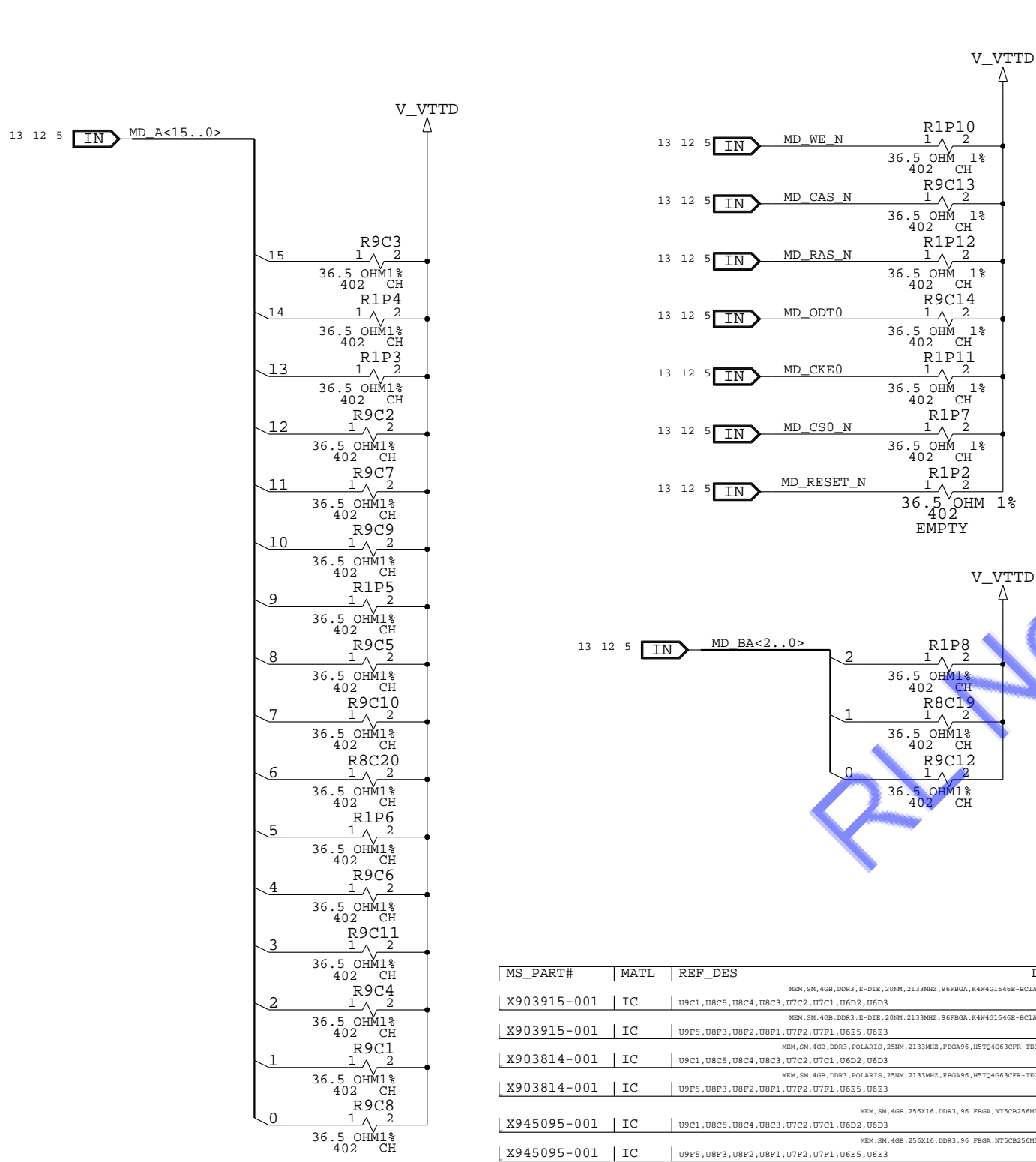




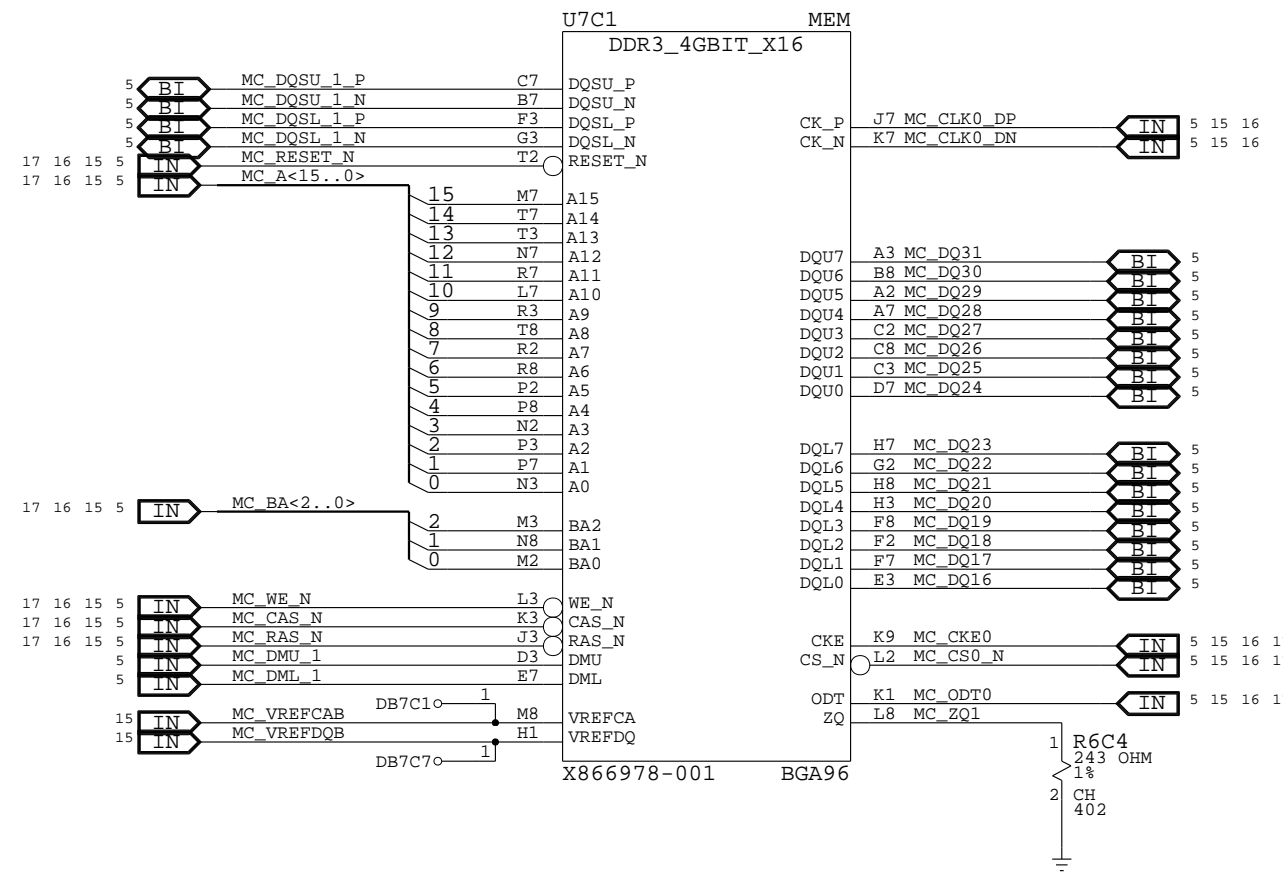
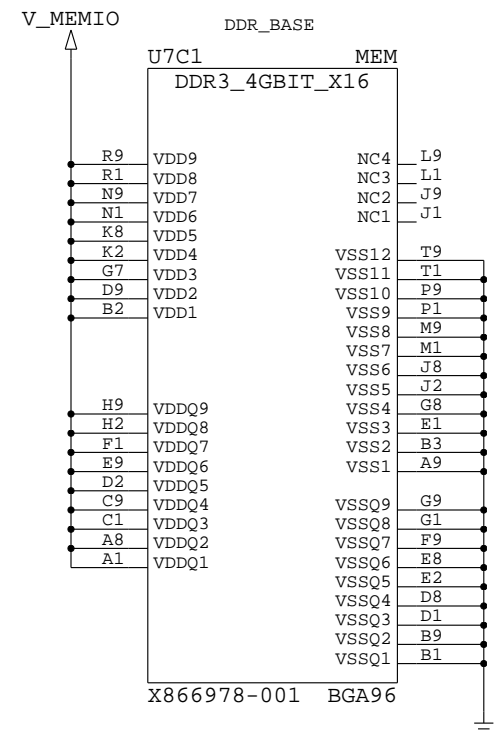
MEMORY: CHANNEL D



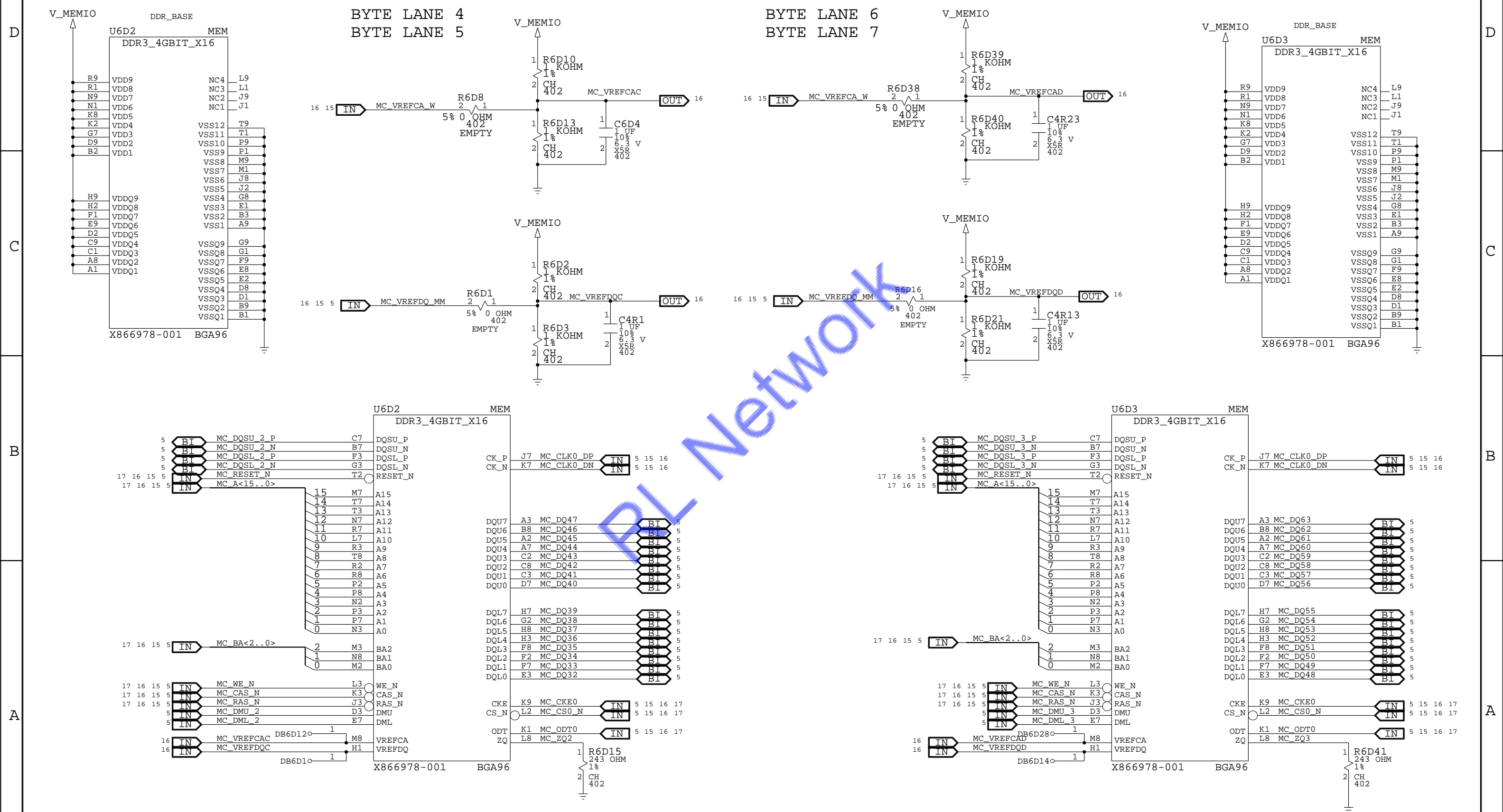
MEMORY: CHANNEL D, DECOUPLING & TERMINATION



8	7	6	5	4	3	2	1
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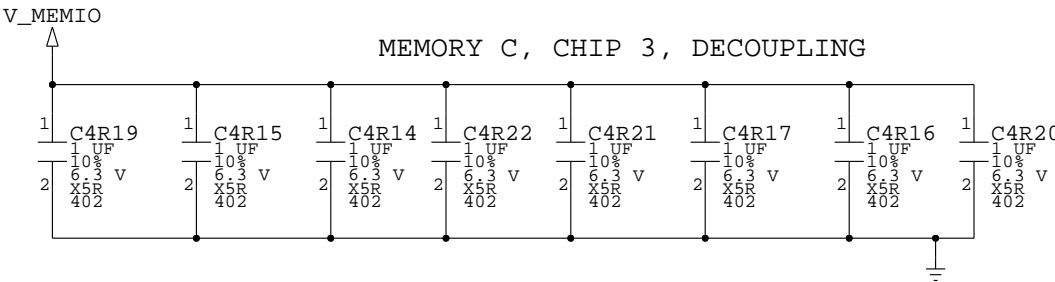
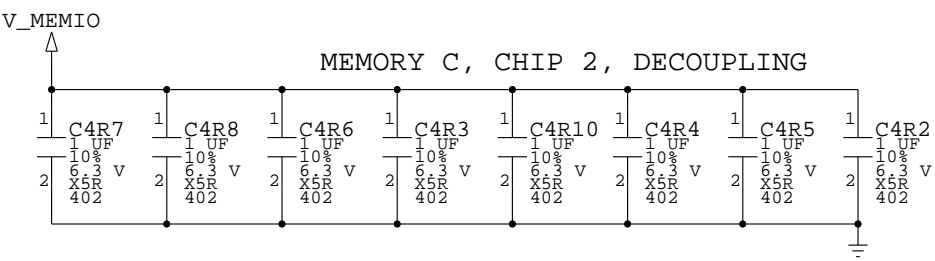
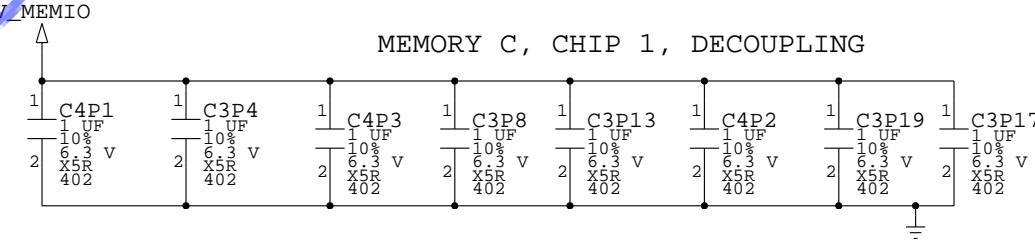
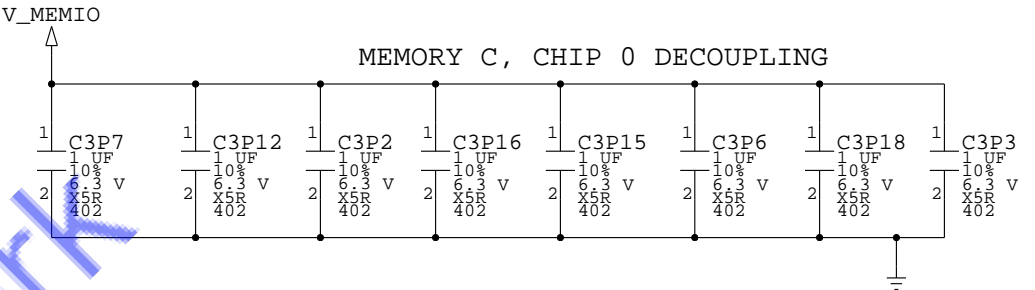
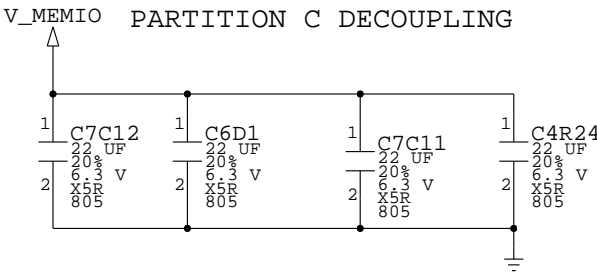
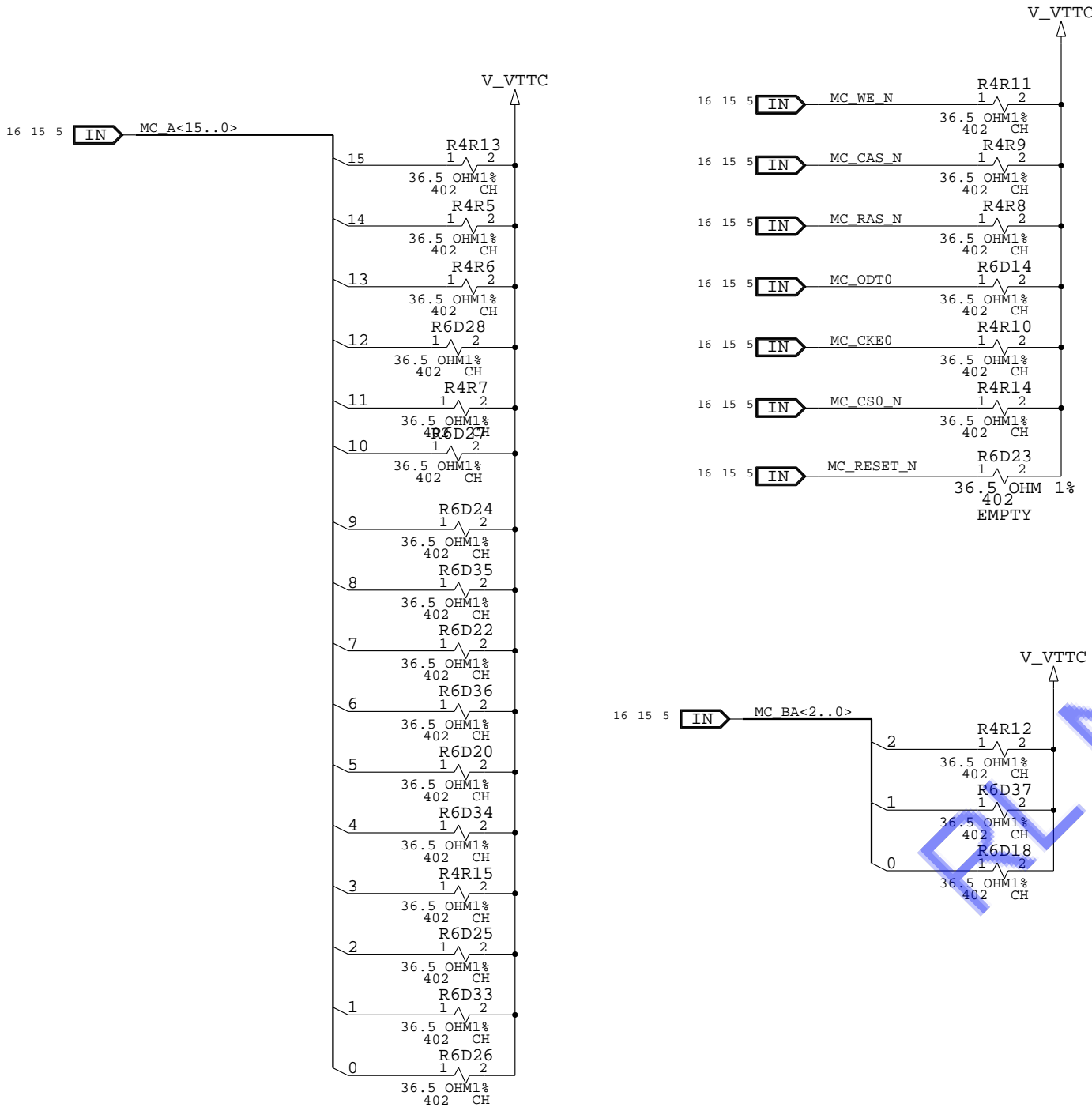


MEMORY: CHANNEL C

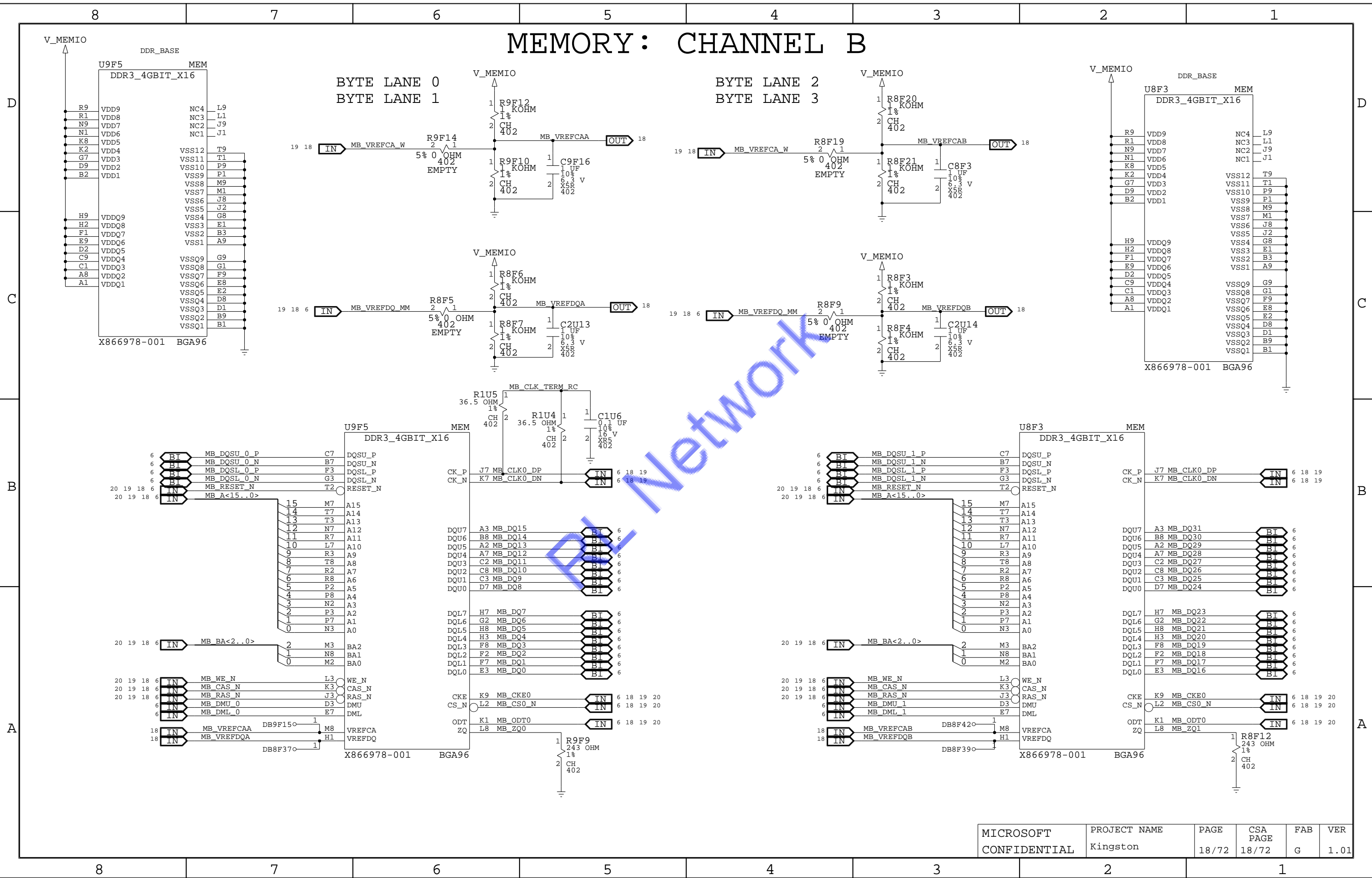




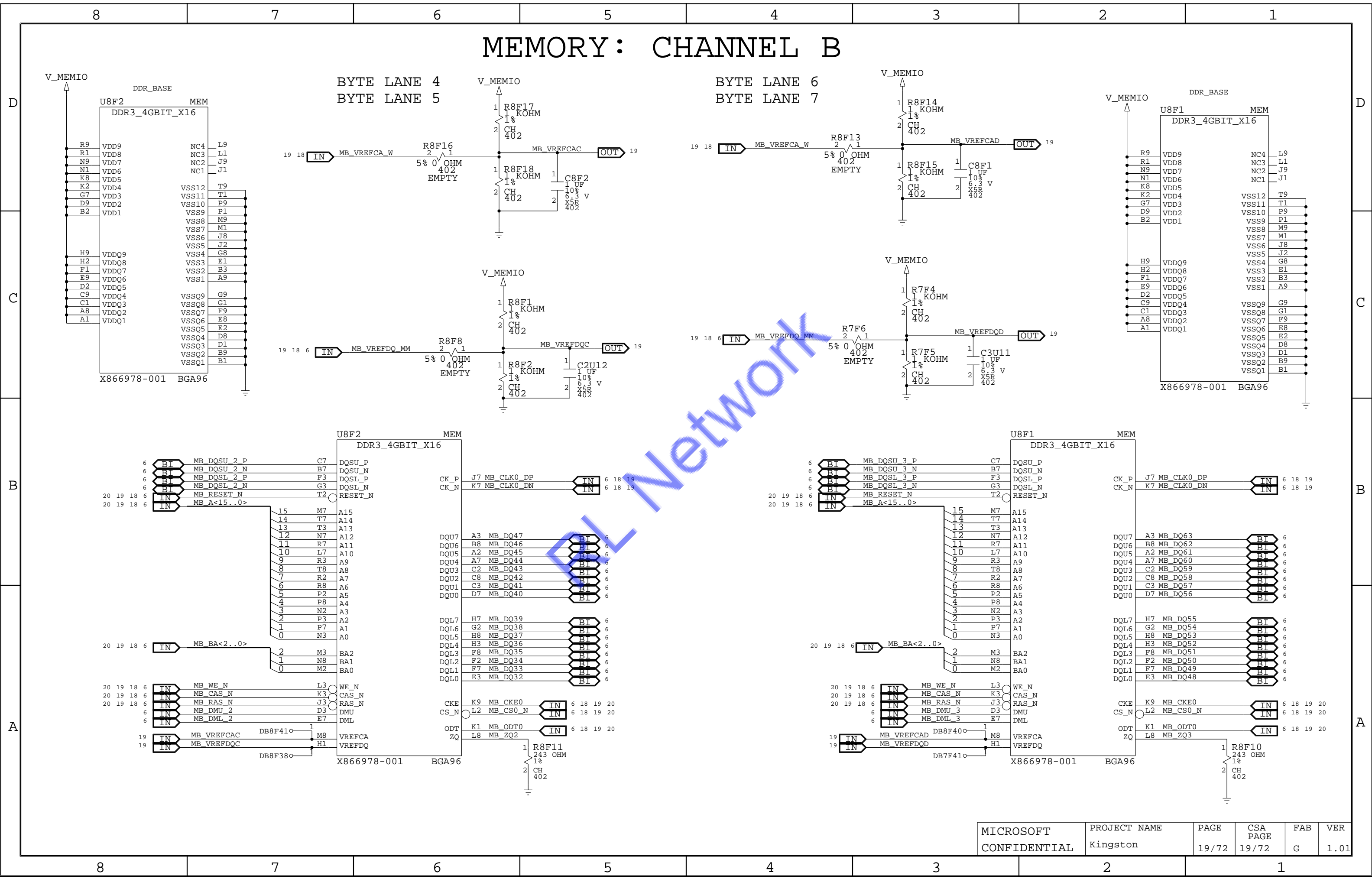
MEMORY: CHANNEL C, DECOUPLING & TERMINATION



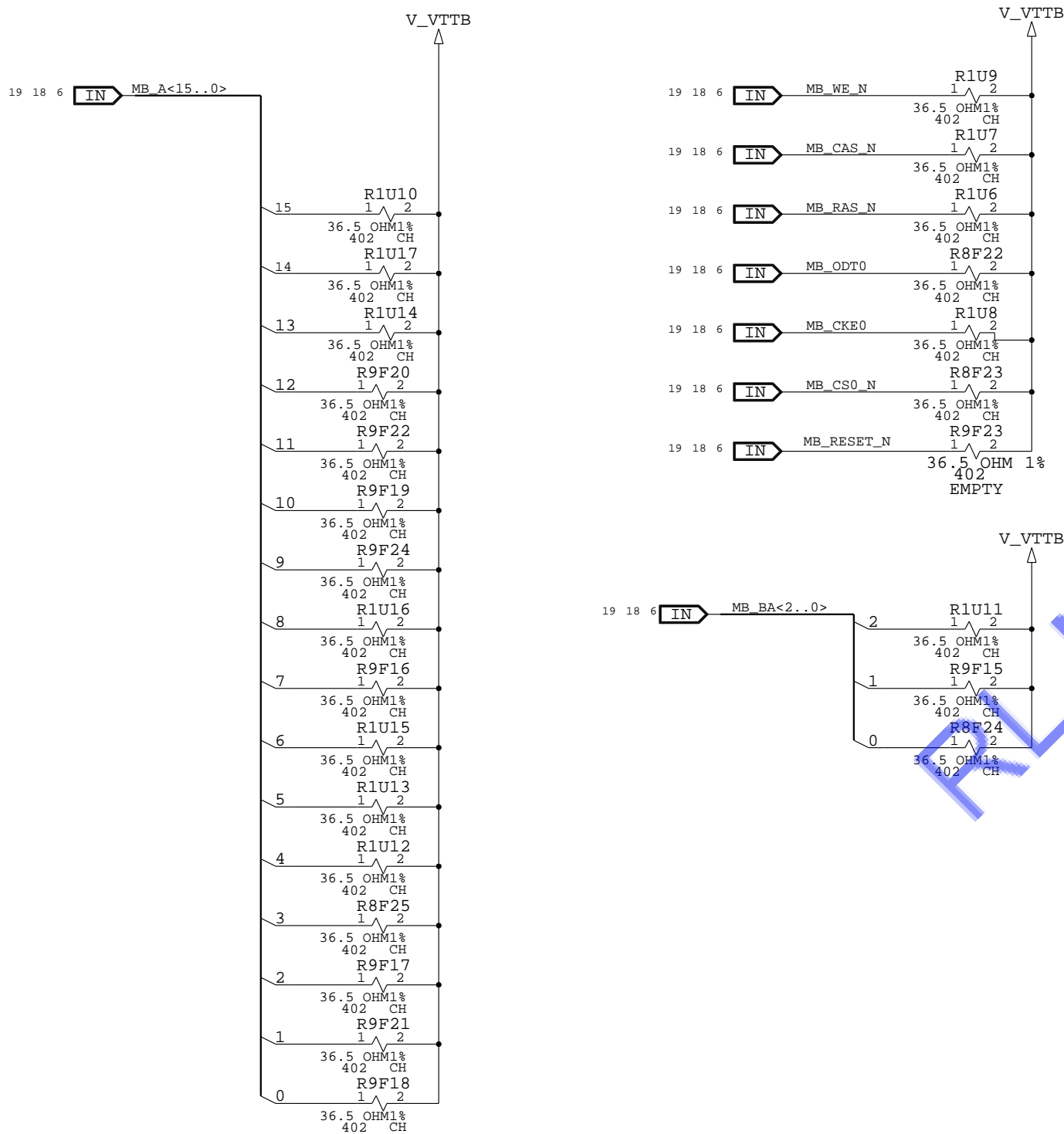
# MEMORY: CHANNEL B



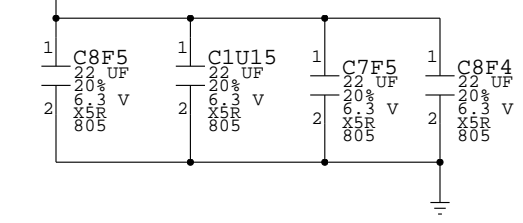
MEMORY : CHANNEL B



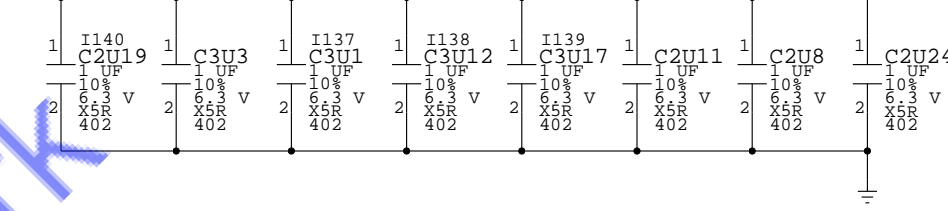
MEMORY: CHANNEL B, DECOUPLING & TERMINATION



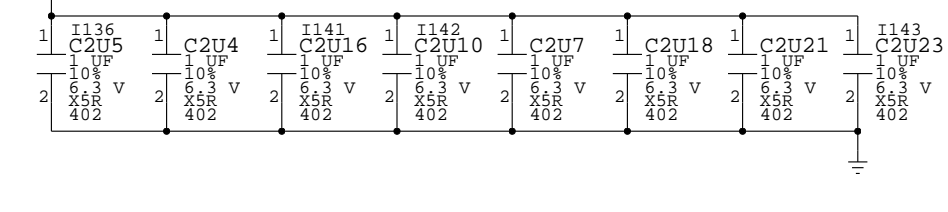
PARTITION B DECOUPLING



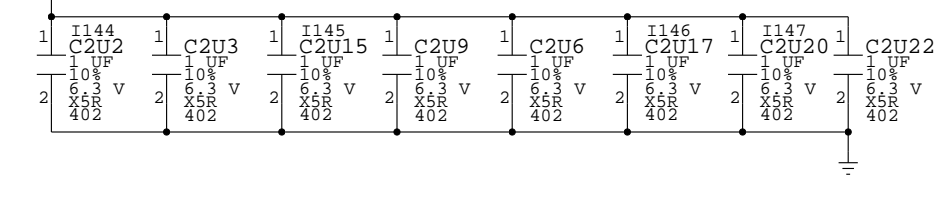
MEMORY B, CHIP 0 DECOUPLING



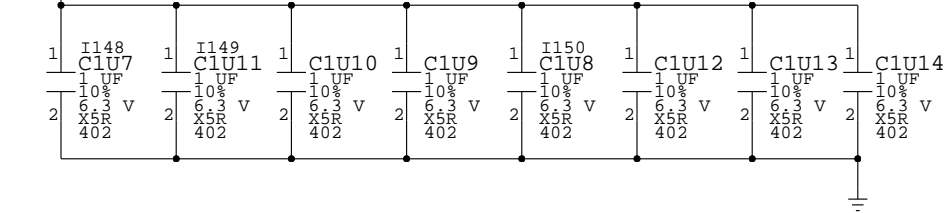
MEMORY B, CHIP 1, DECOUPLING



MEMORY B, CHIP 2, DECOUPLING

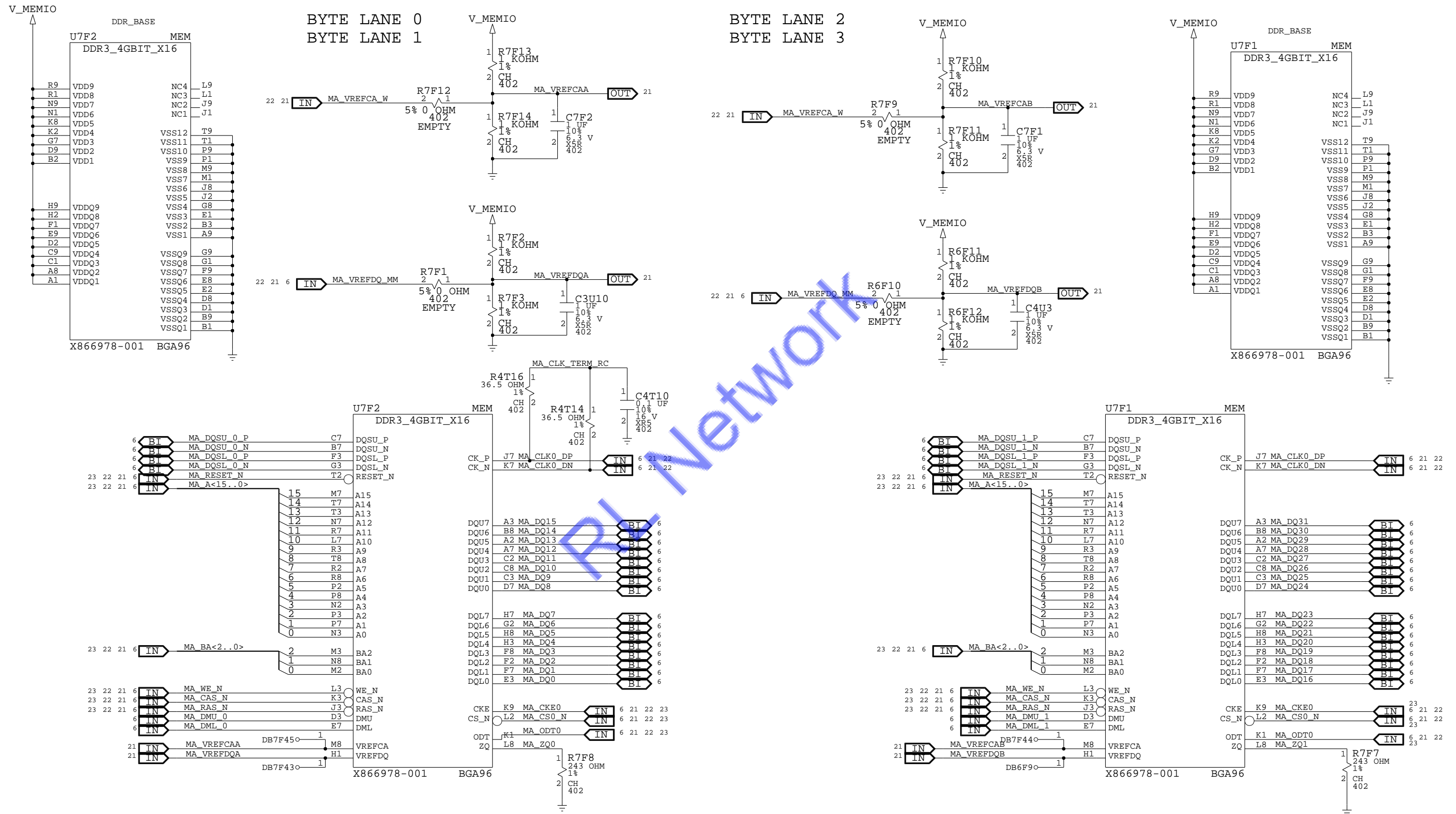


MEMORY B, CHIP 3, DECOUPLING

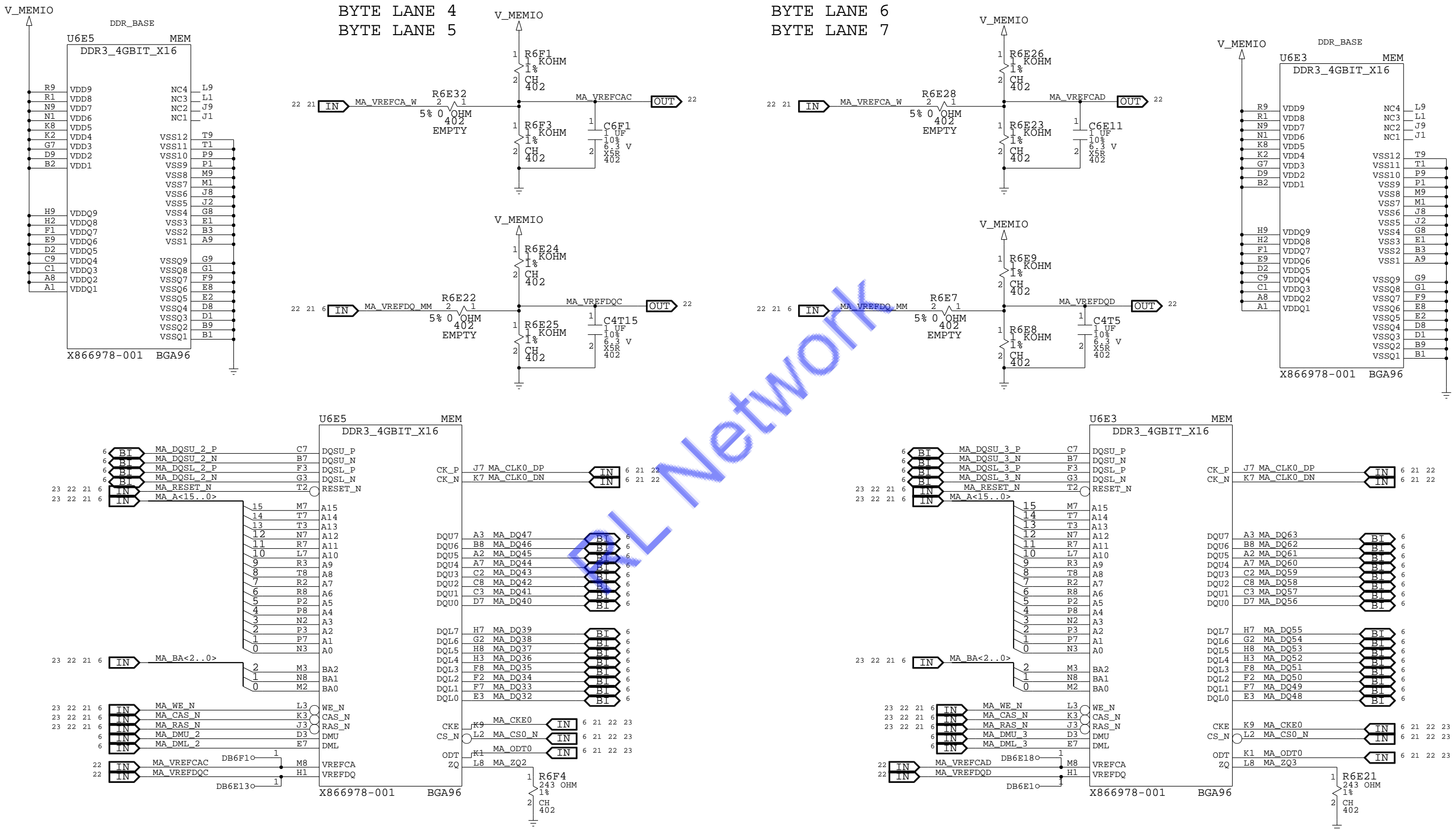




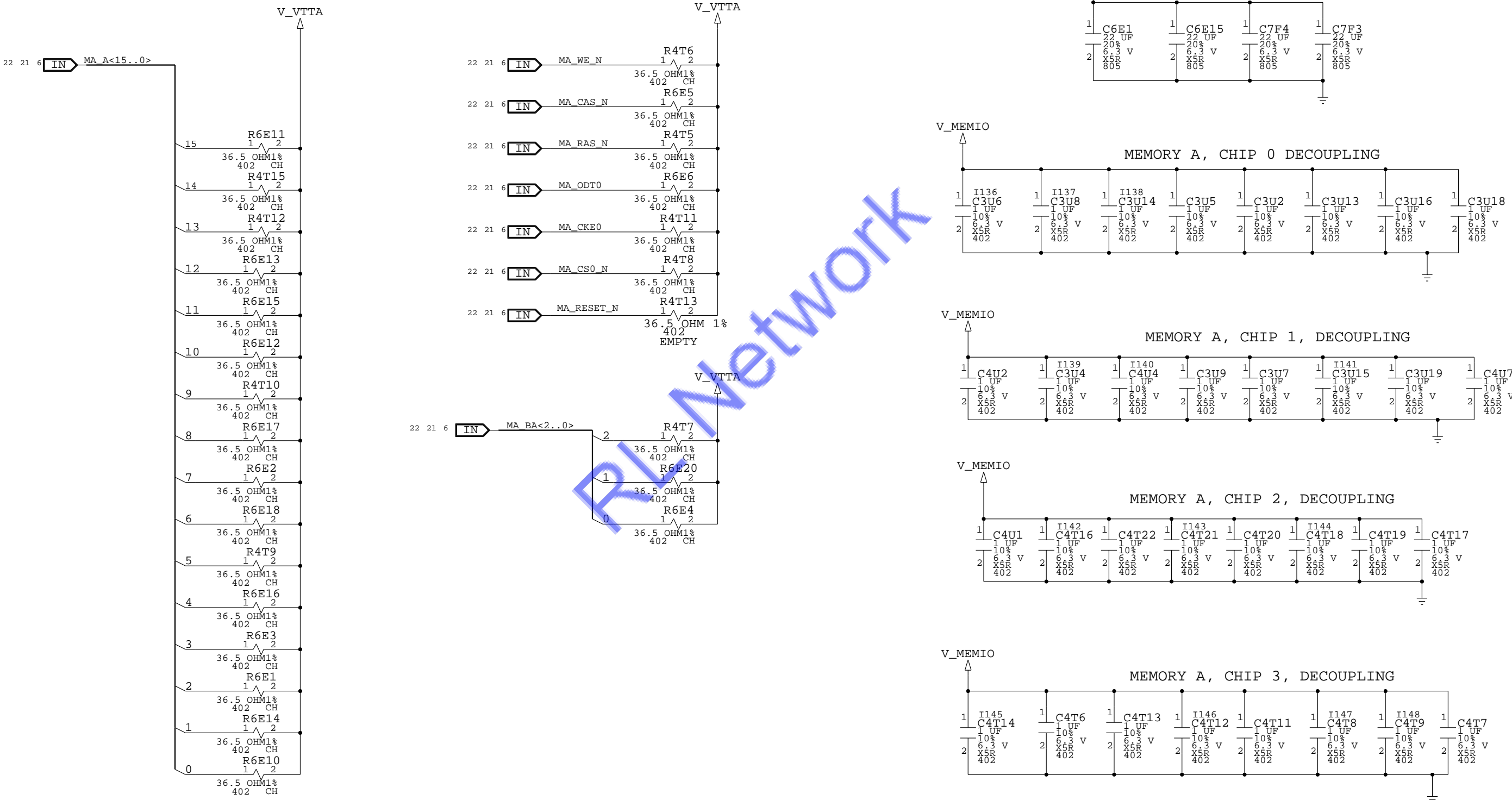
MEMORY: CHANNEL A

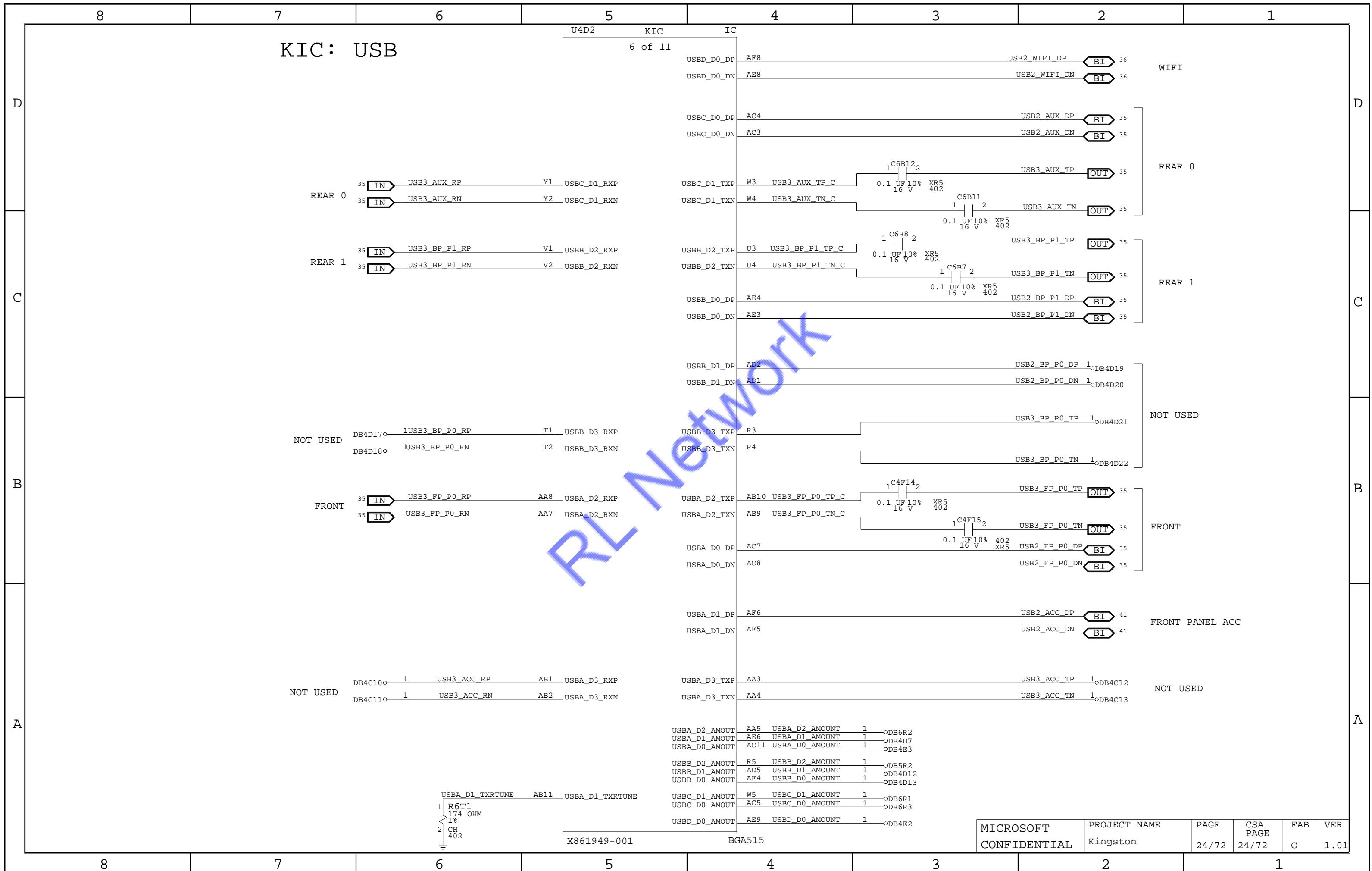


MEMORY: CHANNEL A



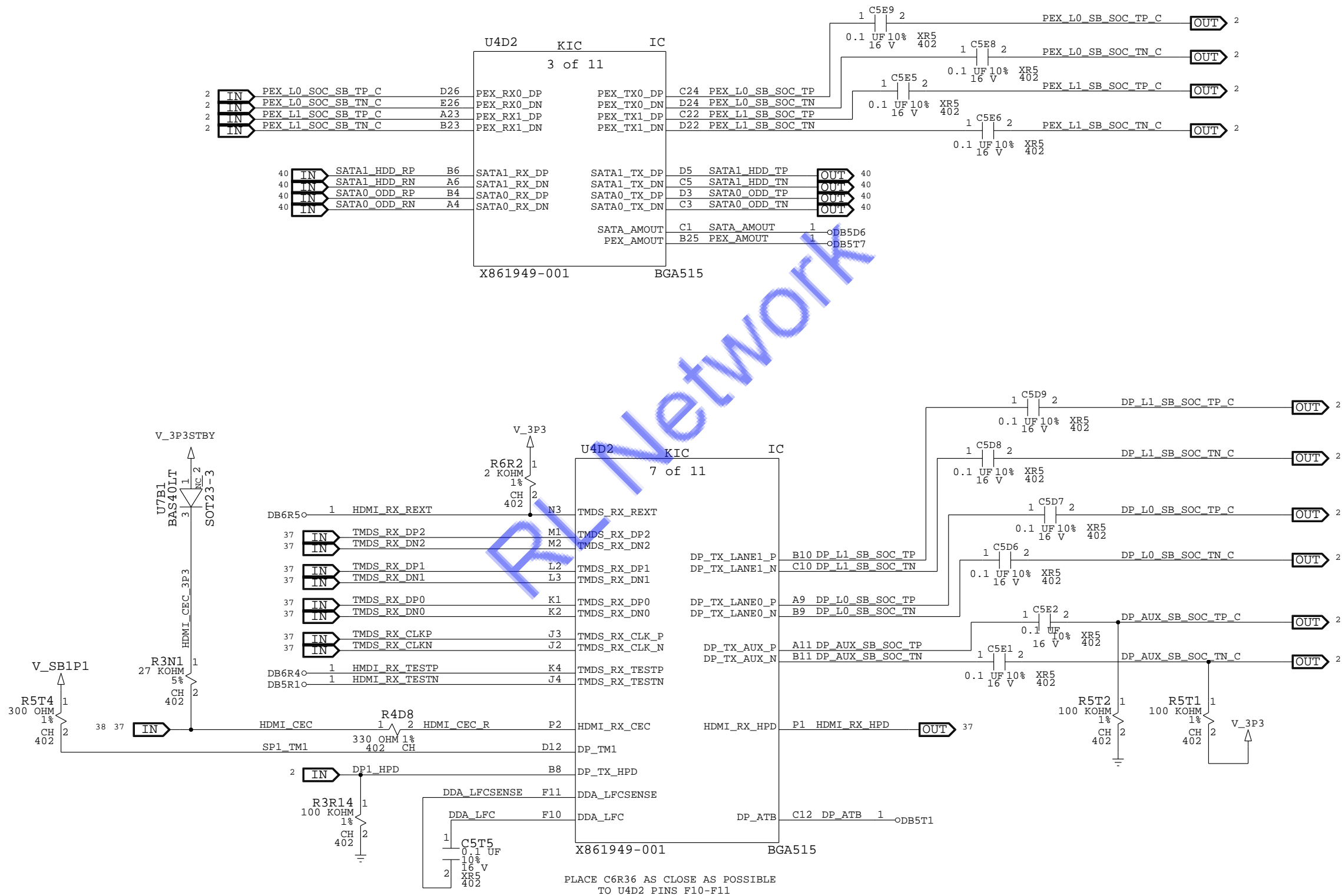
MEMORY: CHANNEL A, DECOUPLING & TERMINATION



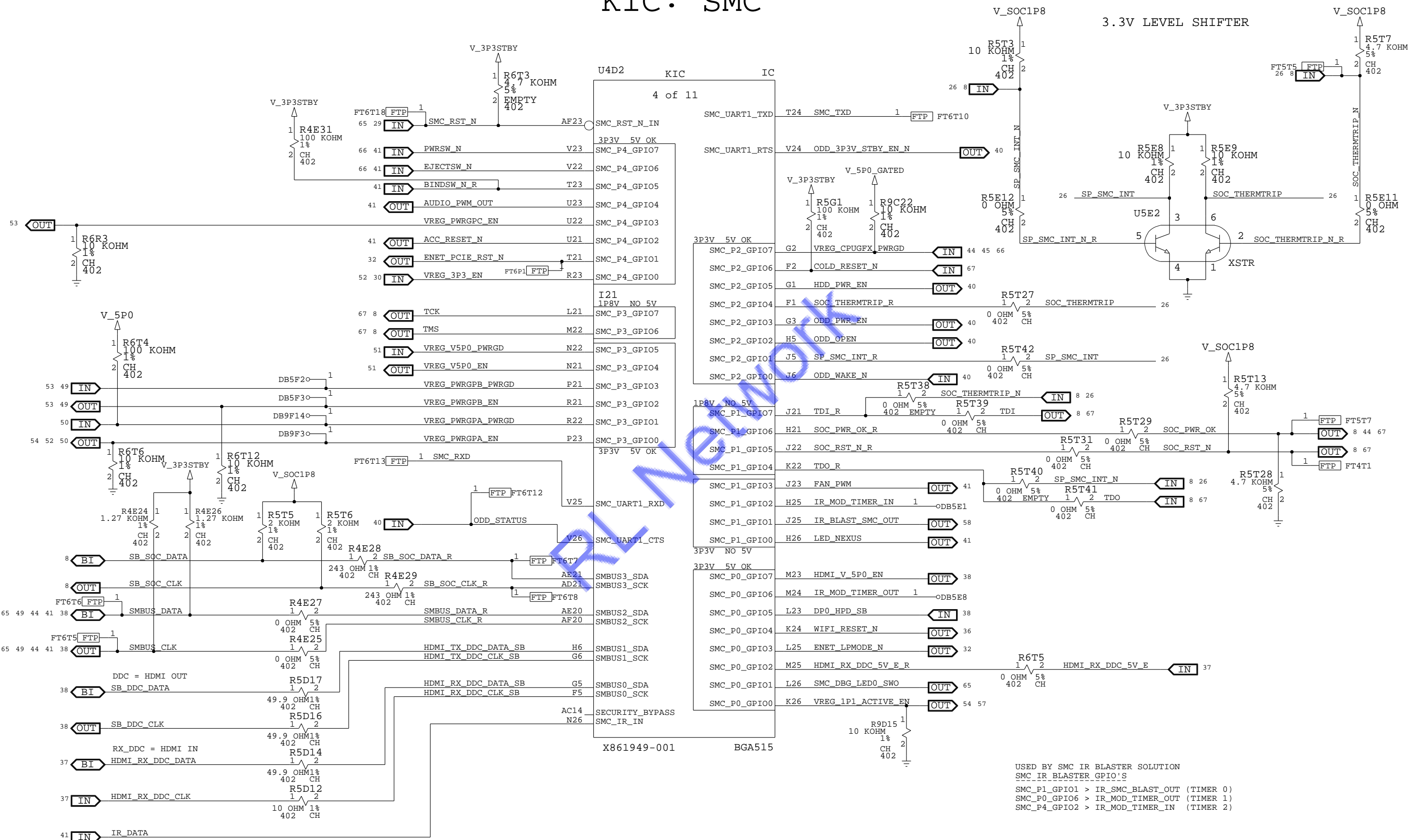




KIC: PCIEX, SATA, VIDEO

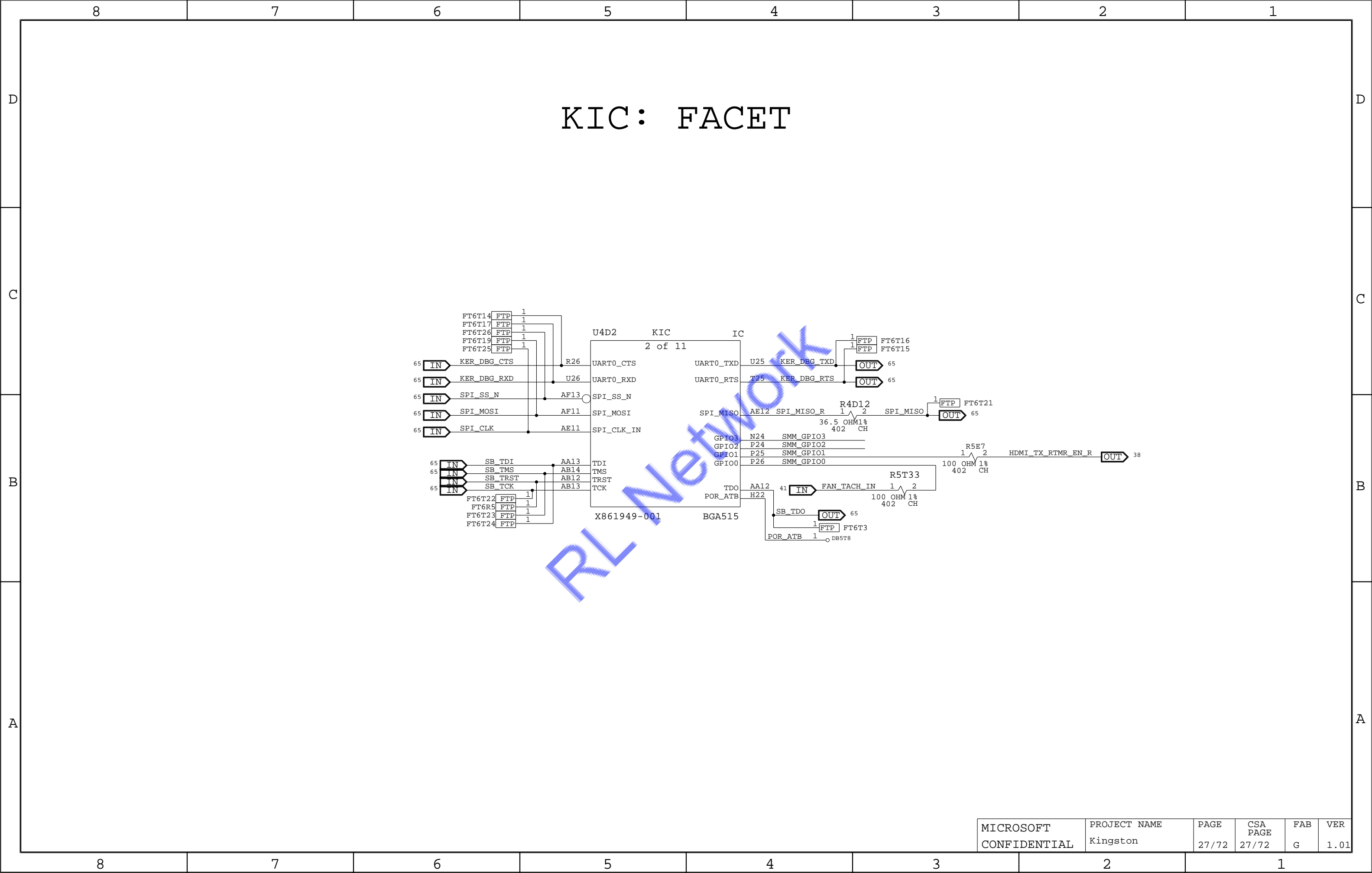


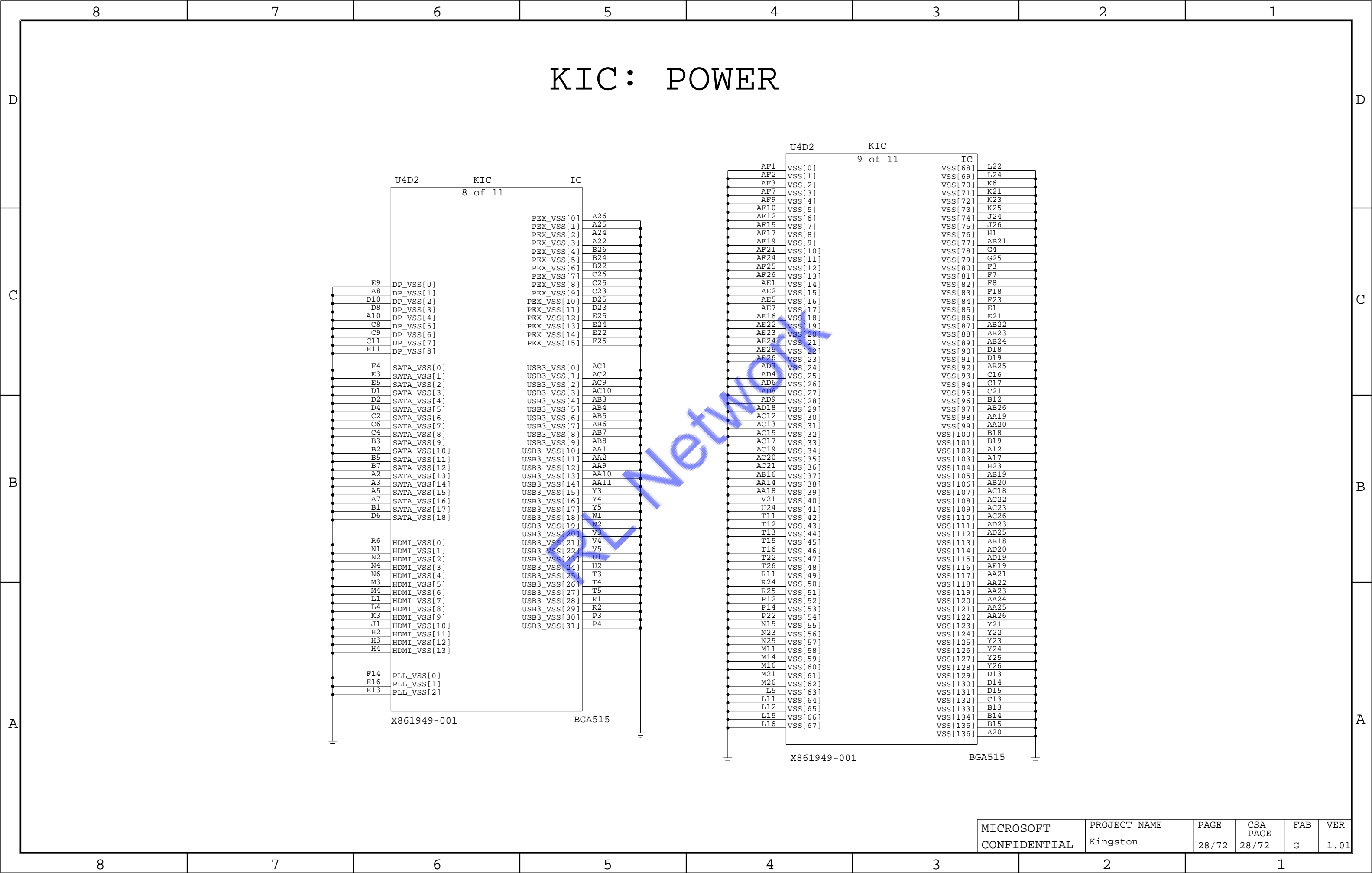
## KIC: SMC



```
USED BY SMC IR BLASTER SOLUTION
SMC_IR_BLASTER_GPIO'S
SMC_P1_GPIO1 > IR_SMC_BLAST_OUT (TIMER 0)
SMC_P0_GPIO6 > IR_MOD_TIMER_OUT (TIMER 1)
SMC_P4_GPIO2 > IR_MOD_TIMER_IN (TIMER 2)
```

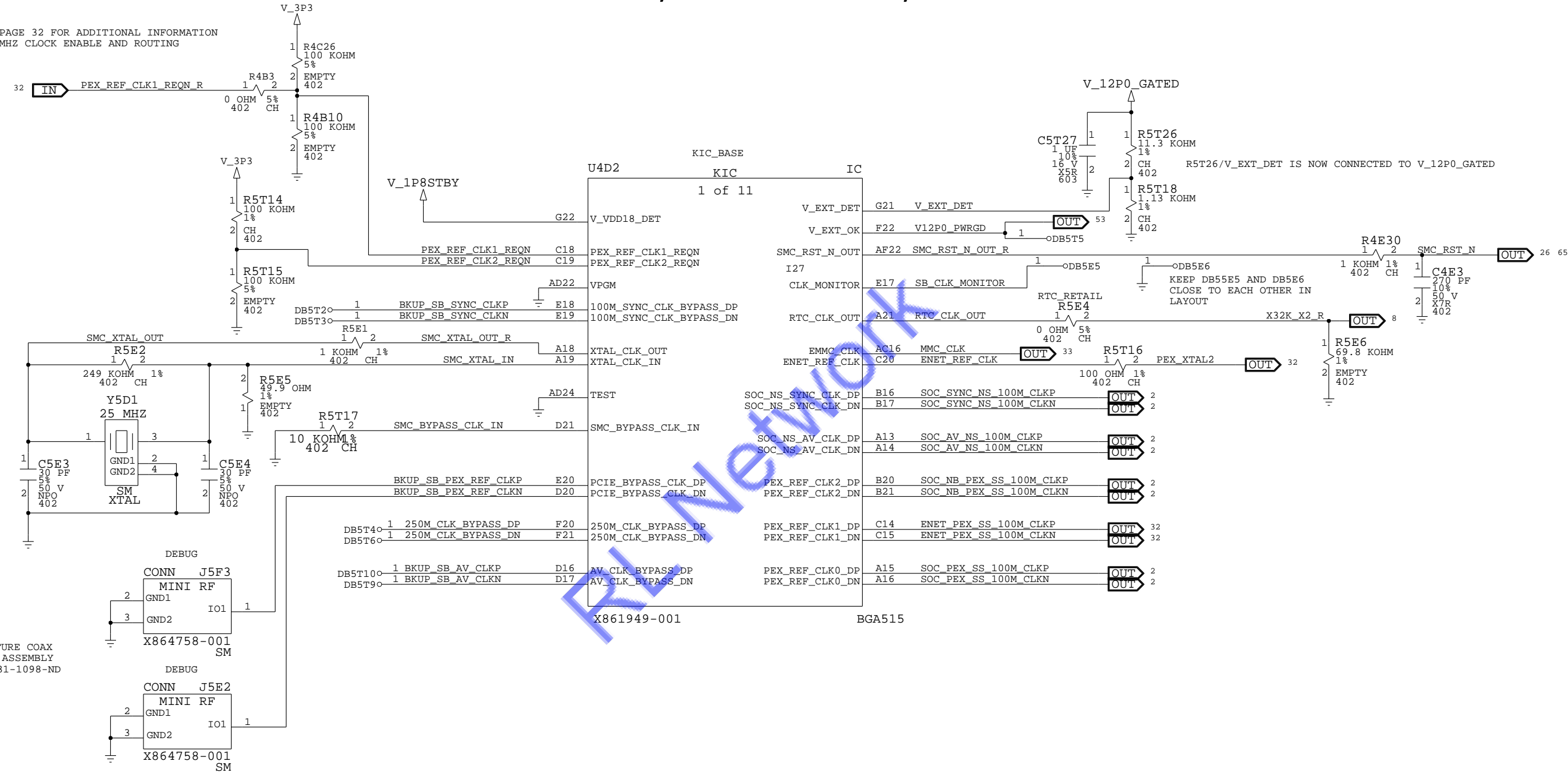
MICROSOFT CONFIDENTIAL	PROJECT NAME Kingston	PAGE 26/72	CSA PAGE 26/72	FAB G	VER 1.01
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KIC: CLOCKS, STRAPPING, POR

SEE PAGE 32 FOR ADDITIONAL INFORMATION  
100 MHZ CLOCK ENABLE AND ROUTING



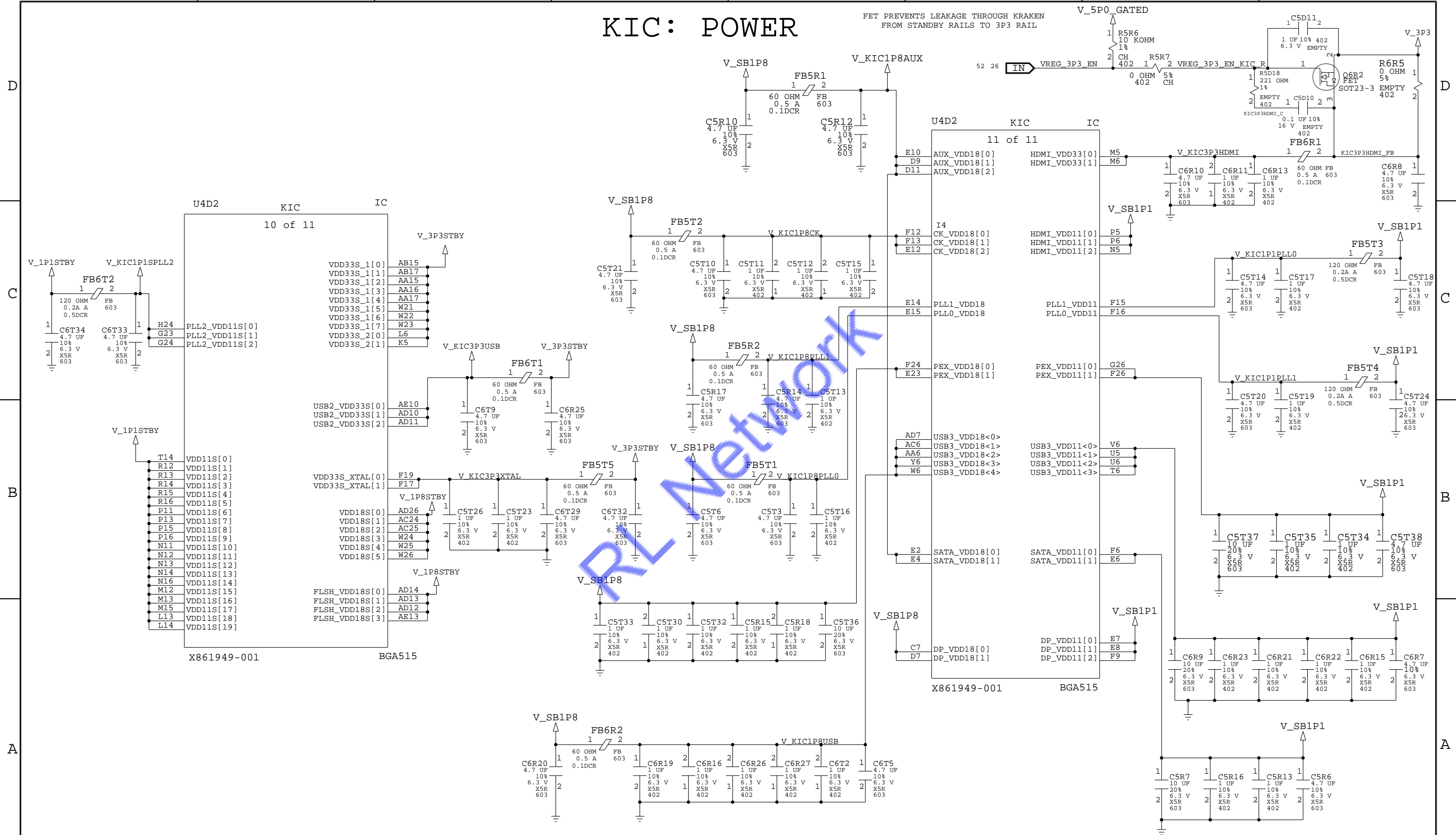
ULTRA MINIATURE COAX  
TO SMA CABLE ASSEMBLY  
DIGIKEY PN: 931-1098-ND

MS_PART#	MATL	REF DES	DESCR.	BOM PROPERTY
X861949-005	IC	U4D2	IC,KRAKEN SB,BGA515	KIC_RETAIL
X861949-003	IC	U4D2	IC,KRAKEN SB,BGA515	KIC_DEV

MICROSOFT CONFIDENTIAL	PROJECT NAME Kingston	PAGE 29/72	CSA PAGE 29/72	FAB G	VER 1.01
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# KIC: POWER

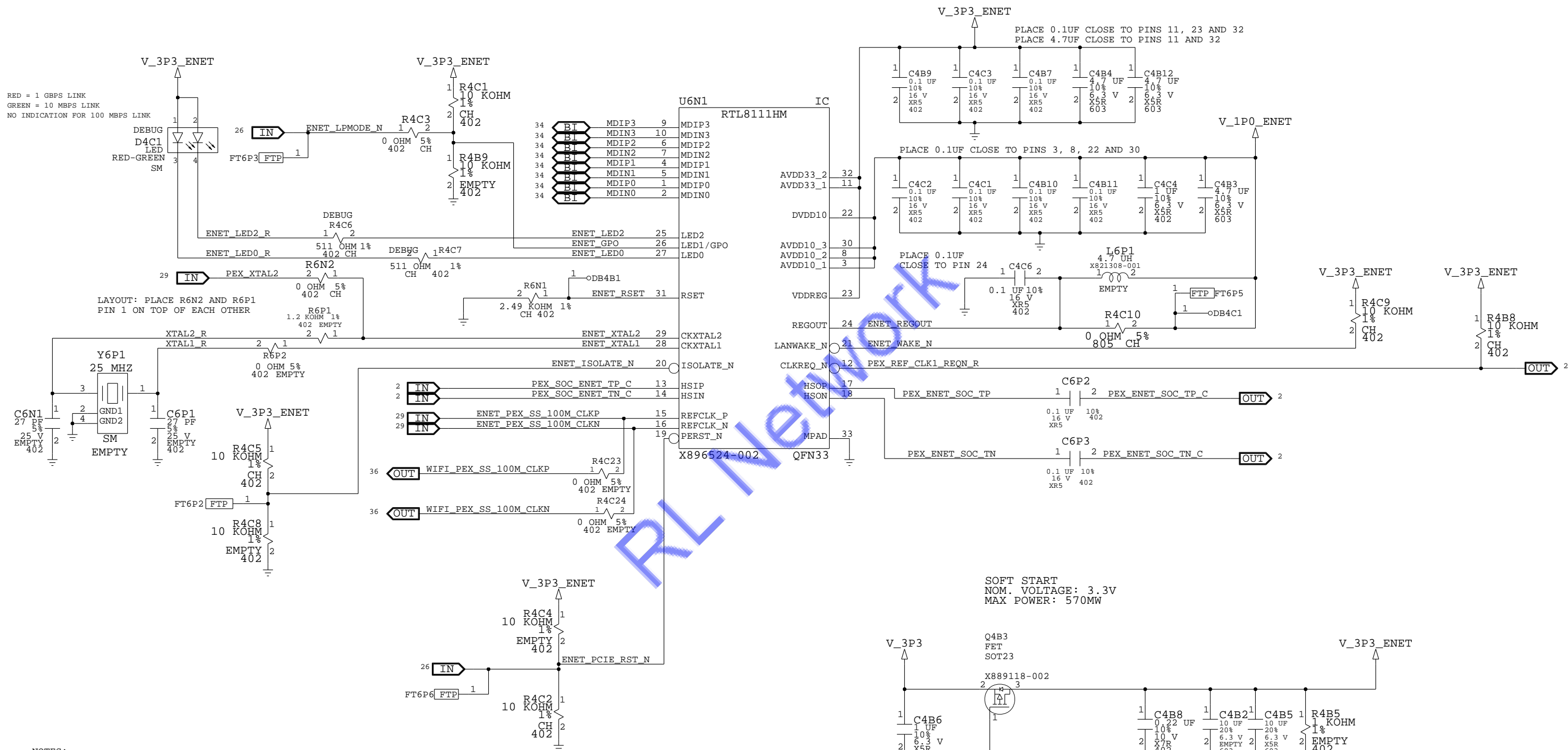


KIC: DECOUPLING

The diagram illustrates the decoupling network for various power planes. The components are organized into columns corresponding to the power planes: V\_1P1STBY, V\_KIC1P8AUX, V\_SB1P1, V\_3P3STBY, V\_1P8STBY, V\_KIC3P3USB, and V\_KIC1P1SPLL2. Each column shows a series of decoupling components (capacitors and resistors) connected to ground. The components are labeled with their values and footprints, such as 4.7 UF 10% 6.3 V X5R 603, 1 C6T1 2, 1 C6T2 2, 1 C6T3 2, 1 C6T4 2, 1 C6T5 2, 1 C6T6 2, 1 C6T7 2, 1 C6T8 2, 1 C6T9 2, 1 C6T10 2, 1 C6T11 2, 1 C6T12 2, 1 C6T13 2, 1 C6T14 2, 1 C6T15 2, 1 C6T16 2, 1 C6T17 2, 1 C6T18 2, 1 C6T19 2, 1 C6T20 2, 1 C6T21 2, 1 C6T22 2, 1 C6T23 2, 1 C6T24 2, 1 C6T25 2, 1 C6T26 2, 1 C6T27 2, 1 C6T28 2, 1 C6T29 2, 1 C6T30 2, 1 C6T31 2, 1 C6T32 2, 1 C6T33 2, 1 C6T34 2, 1 C6T35 2, 1 C6T36 2, 1 C6T37 2, 1 C6T38 2, 1 C6T39 2, 1 C6T40 2, 1 C6T41 2, 1 C6T42 2, 1 C6T43 2, 1 C6T44 2, 1 C6T45 2, 1 C6T46 2, 1 C6T47 2, 1 C6T48 2, 1 C6T49 2, 1 C6T50 2, 1 C6T51 2, 1 C6T52 2, 1 C6T53 2, 1 C6T54 2, 1 C6T55 2, 1 C6T56 2, 1 C6T57 2, 1 C6T58 2, 1 C6T59 2, 1 C6T60 2, 1 C6T61 2, 1 C6T62 2, 1 C6T63 2, 1 C6T64 2, 1 C6T65 2, 1 C6T66 2, 1 C6T67 2, 1 C6T68 2, 1 C6T69 2, 1 C6T70 2, 1 C6T71 2, 1 C6T72 2, 1 C6T73 2, 1 C6T74 2, 1 C6T75 2, 1 C6T76 2, 1 C6T77 2, 1 C6T78 2, 1 C6T79 2, 1 C6T80 2, 1 C6T81 2, 1 C6T82 2, 1 C6T83 2, 1 C6T84 2, 1 C6T85 2, 1 C6T86 2, 1 C6T87 2, 1 C6T88 2, 1 C6T89 2, 1 C6T90 2, 1 C6T91 2, 1 C6T92 2, 1 C6T93 2, 1 C6T94 2, 1 C6T95 2, 1 C6T96 2, 1 C6T97 2, 1 C6T98 2, 1 C6T99 2, 1 C6T100 2. The components are connected to ground through a series of resistors and capacitors. A large blue watermark 'RLNetwork' is visible across the center of the layout.

MICROSOFT	PROJECT NAME	PAGE	CSA	FAB	VER
CONFIDENTIAL	Kingston	31/72	PAGE	G	1.01

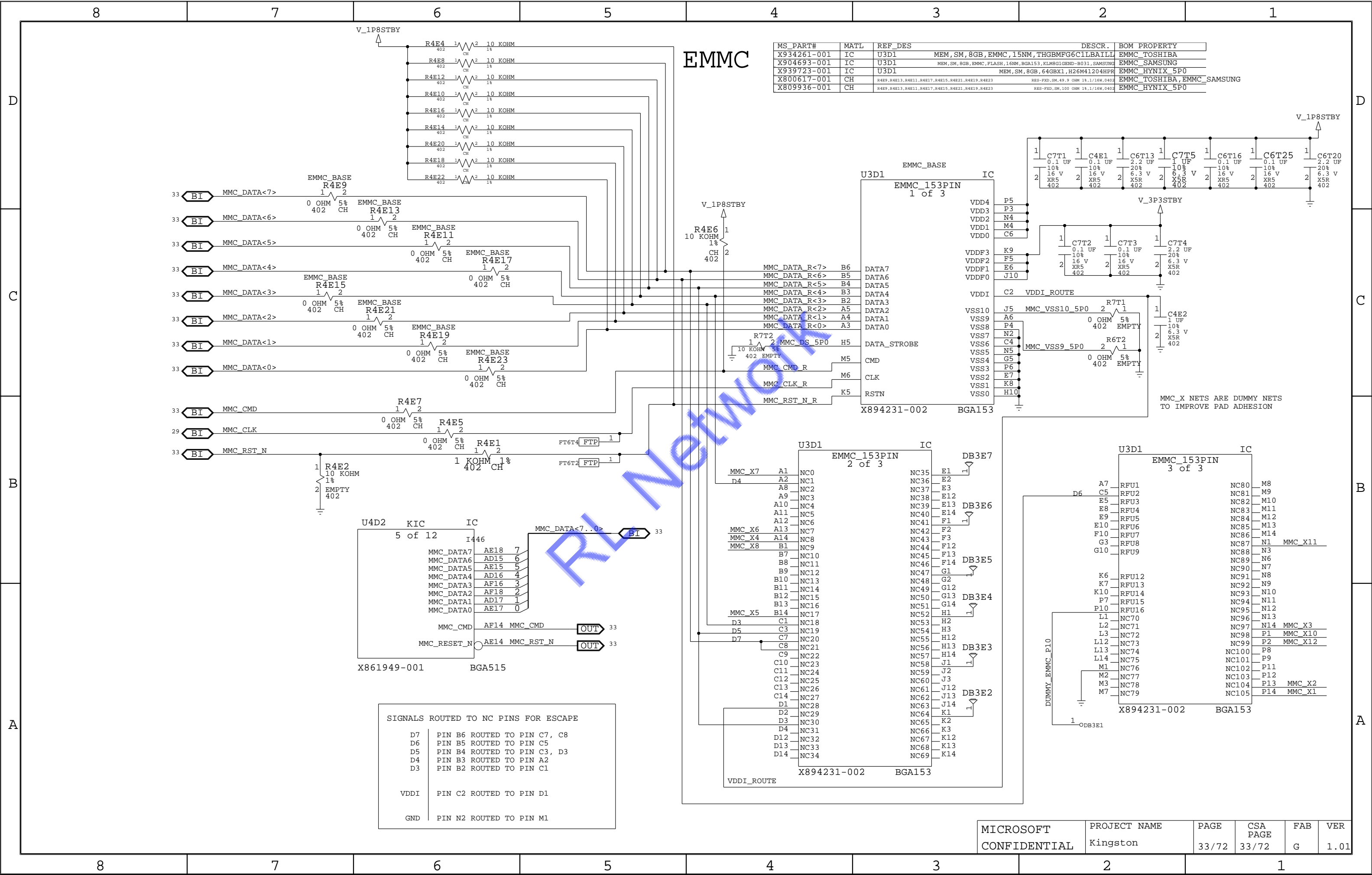
ETHERNET CONTROLLER



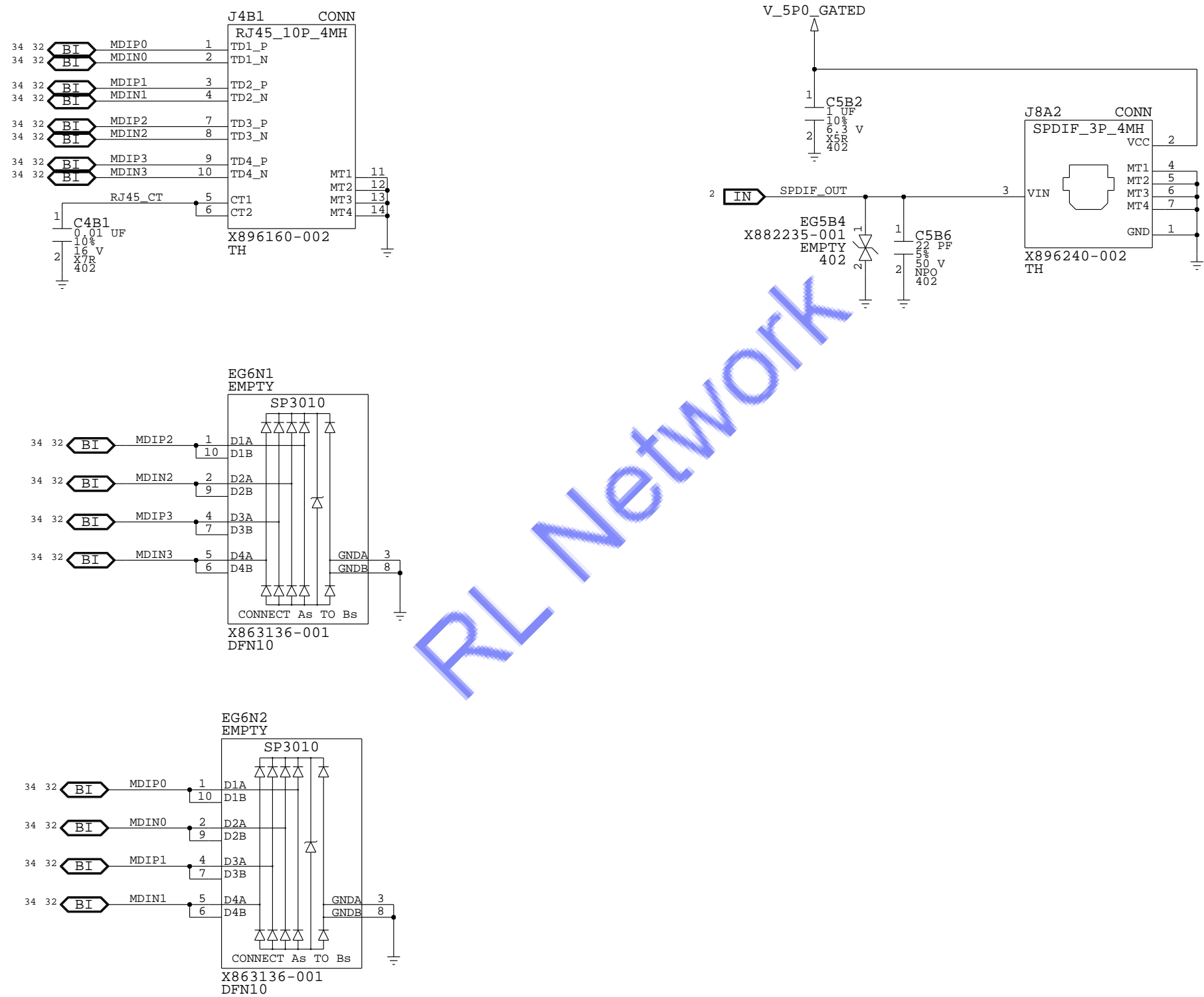
- NOTES:
1. THE RTL8111HM IS CONFIGURED FROM REALTEK WITH EFUSE "ENABLE LAN DISABLE" MODE SET, WHICH PROVIDES DEFAULT SUPPORT FOR SIGNAL ENET\_LPMODE\_N. THIS FEATURE CAN BE OVERRIDDEN BY SOFTWARE
  2. TO SUPPORT A PCIE WIFI INTERFACE (J3C1), THE FOLLOWING BOM CHANGES ARE NEEDED:
    - A: POPULATE R4C23 AND R4C24, WHICH WILL SEND THE 100 MHZ CLOCK TO THE WIFI INTERFACE. IN ADDITION, IT IS CRITICAL THAT EACH LEG OF THE CLOCK BE TERMINATED AT THE FAR END INTO 50 OHMS.
    - B: ON PAGE 2, POPULATE AC COUPLING CAPS C6P6 AND C6P7
    - C: FOR PRELIMINARY DEVELOPMENT TESTING, NO OTHER BOM CHANGES ARE REQUIRED. THE ETHERNET CONTROLLER WILL MANAGE THE ENABLING OF THE 100 MHZ CLOCK.
    - D: FOR PRODUCTION RETAIL, ON PAGE 29 REMOVE R4B3 AND POPULATE R4C26. THIS CHANGE WILL REQUIRE MODIFIED SMC FIRMWARE TO EXPLICITLY ENABLE THE 100 MHZ CLOCK.

SOFT START  
NOM. VOLTAGE: 3.3V  
MAX POWER: 570MW

MICROSOFT CONFIDENTIAL	PROJECT NAME Kingston	PAGE 32/72	CSA PAGE 32/72	FAB G	VER 1.01
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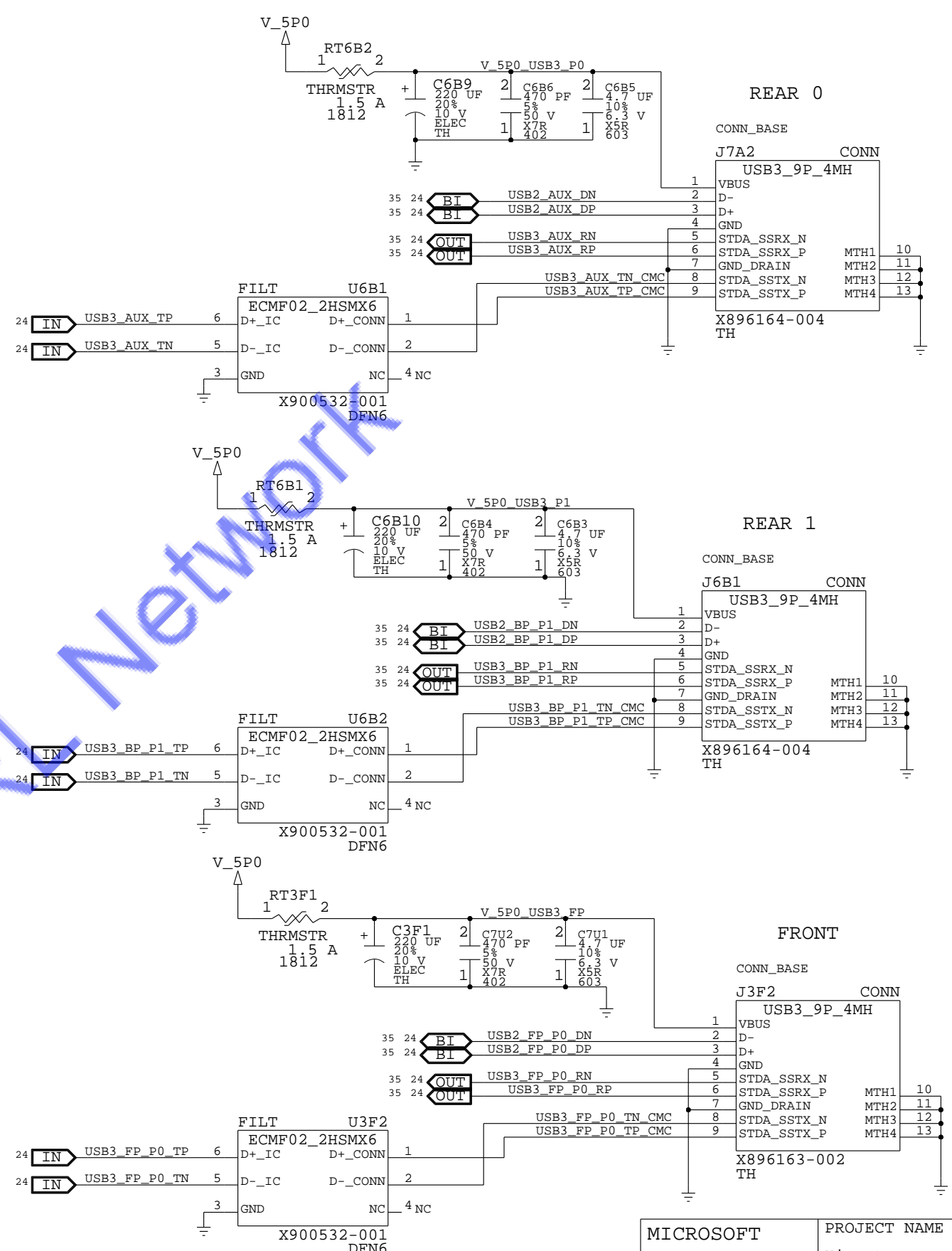
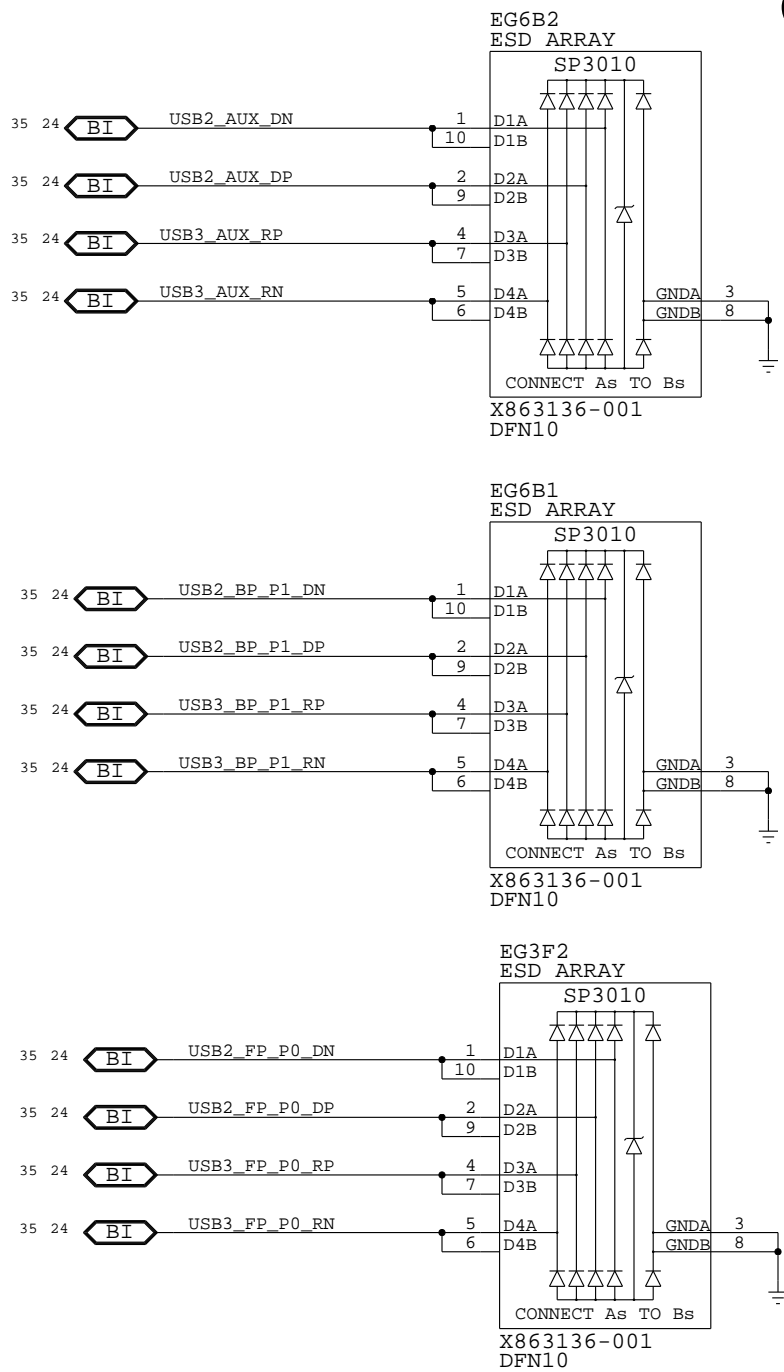


CONN: RJ45 ,TOSLINK



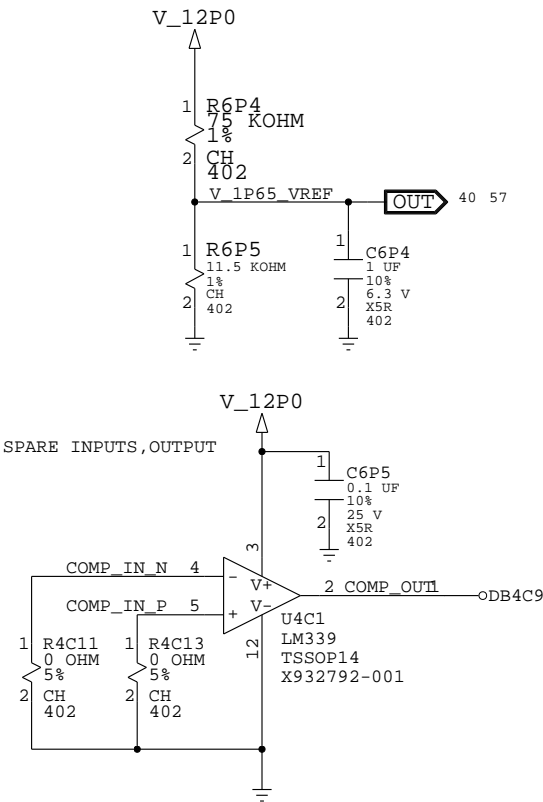


CONN: USB (FRONT & REAR)

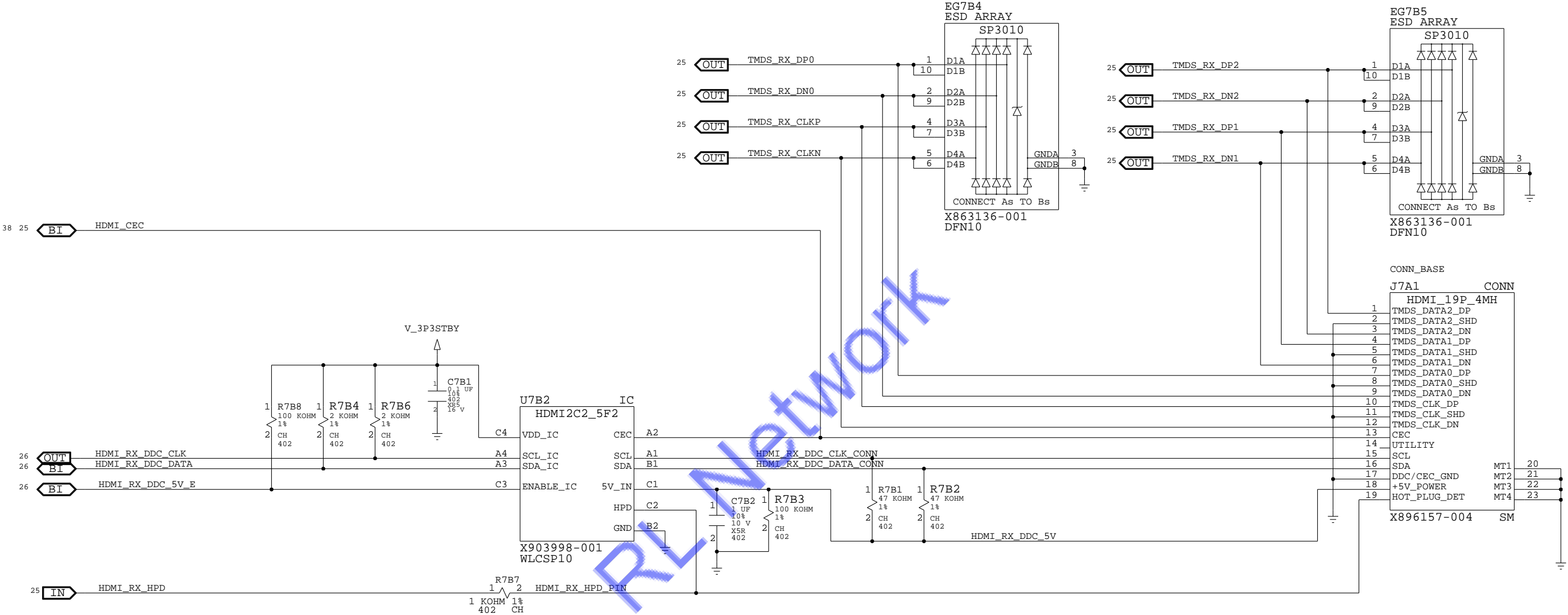


MS_PART#	MATL	REF_DES	DESCR.	BOM PROPERTY
X896164-004	CONN	J7A2,J6B1	CONN-USB,TH,009,FEMALE,USB3-A,BLACK NI, KGS	USB_REAR_FOXC_BLACK
X896164-003	CONN	J7A2,J6B1	CONN-USB,SM,009,FEMALE,USB3-A,PLAIN NI, KGS	USB_REAR_FOXC_PLAIN

MS_PART#	MATL	REF_DES	DESCR.	BOM PROPERTY
X896163-004	CONN	J3F2	CONN-USB,TH,009,FEMALE,FRONT,USB3-A,BLACK NICKEL, KGS	USB_FRONT_FOXC
X907318-002	CONN	J3F2	CONN-USB,TH,009,FEMALE,FRONT,USB3-A,KGS,(QUAL-AMPHENOL)	USB_FRONT_AMPH



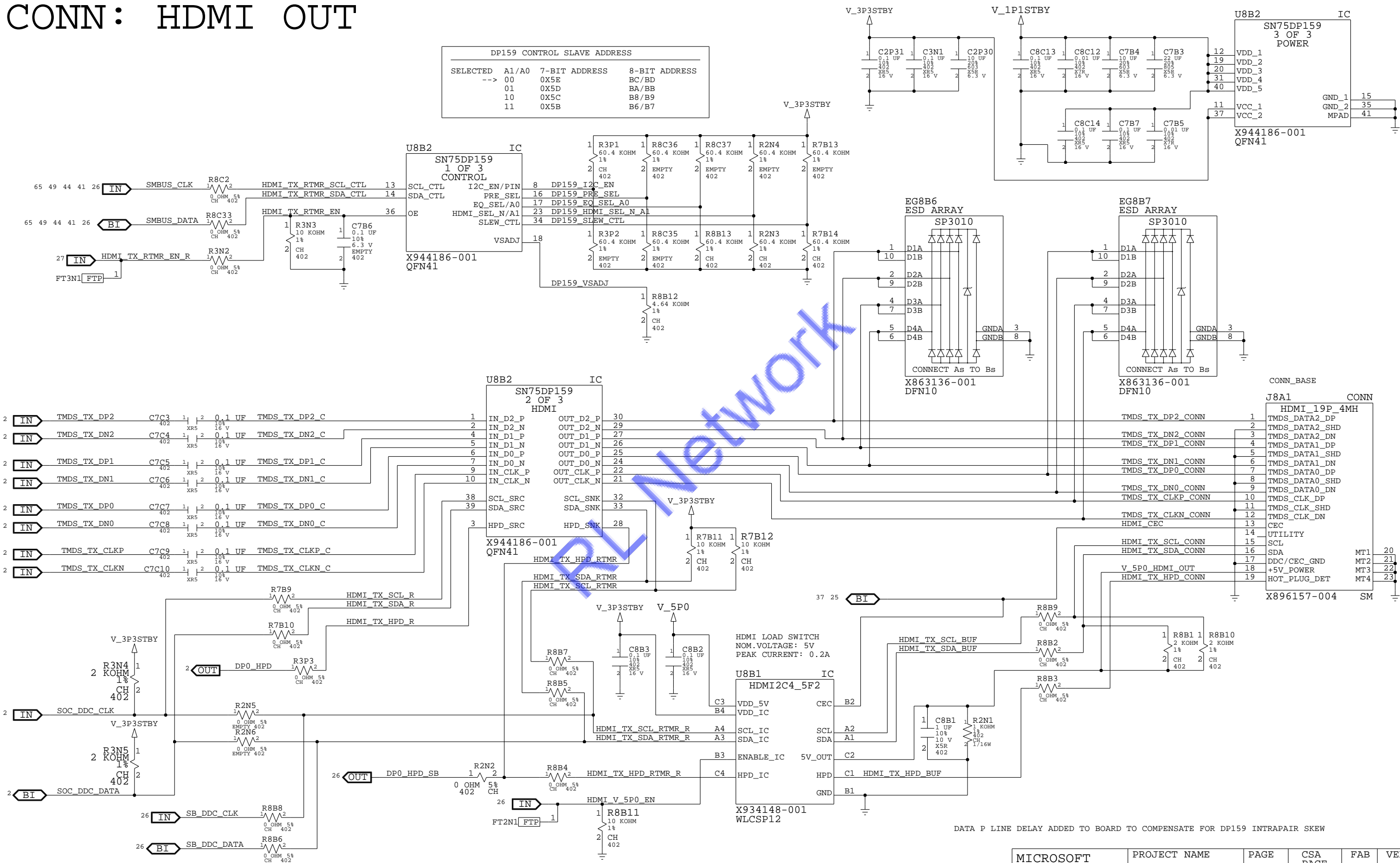
CONN: HDMI IN



MS_PART#	MATL	REF_DES	DESCR.	BOM PROPERTY
X896157-006	CONN	J7A1,J8A1	CONN-HDMI, SM, 019, FEMALE, W/ EMI FLANGES, BLACK NI, KGS	HDMI_FOXC_BLACK
X896157-005	CONN	J7A1,J8A1	CONN-HDMI, SM, 019, FEMALE, W/ EMI FLANGES, PLAIN NI, KGS	HDMI_FOXC_PLAIN

# CONN: HDMI OUT

DP159 CONTROL SLAVE ADDRESS			
SELECTED	A1/A0	7-BIT ADDRESS	8-BIT ADDRESS
-->	00	0X5E	BC/BD
	01	0X5D	BA/BB
	10	0X5C	B8/B9
	11	0X5B	B6/B7



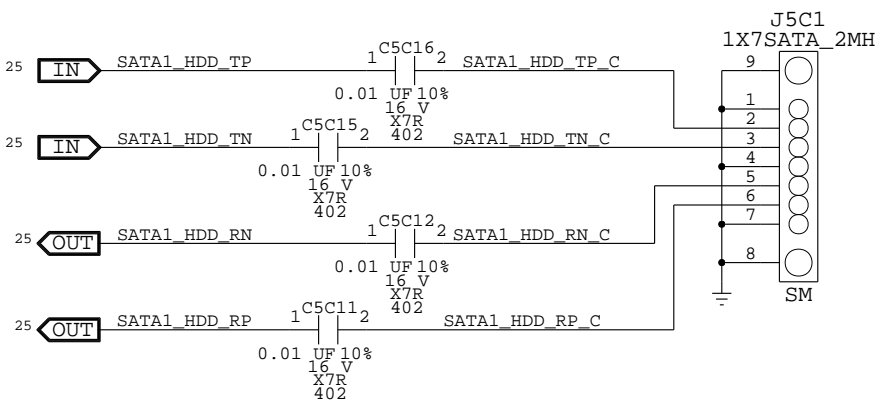
MICROSOFT	PROJECT NAME	PAGE	CSA	FAB	VER
CONFIDENTIAL	Kingston	38/72	PAGE	G	1.01

8		7		6		5		4		3		2		1	
CONN: HDMI SUPPORT															
D														D	
C														C	
B														B	
A														A	
8		7		6		5		4		3		2		1	

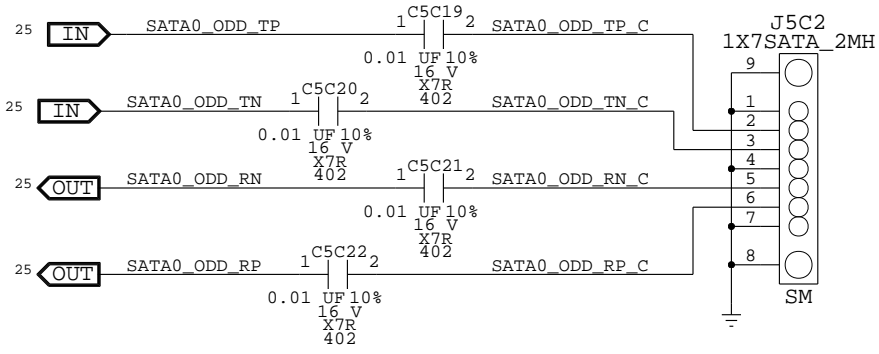


# CONN: ODD & HDD

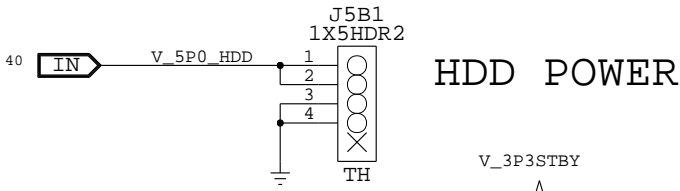
## HDD SATA



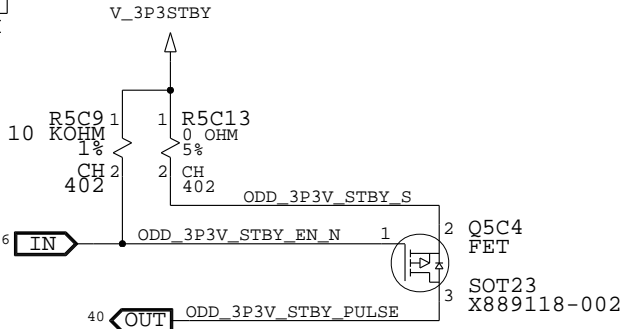
## ODD SATA



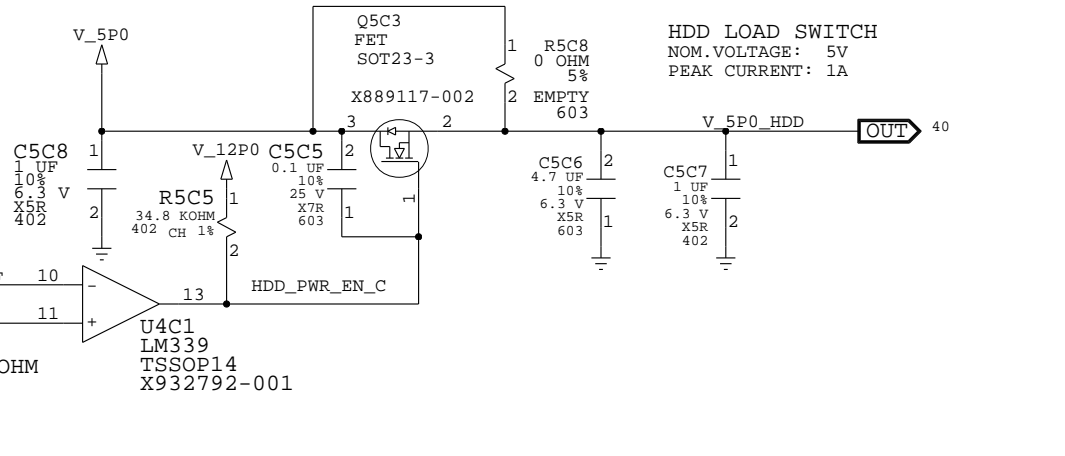
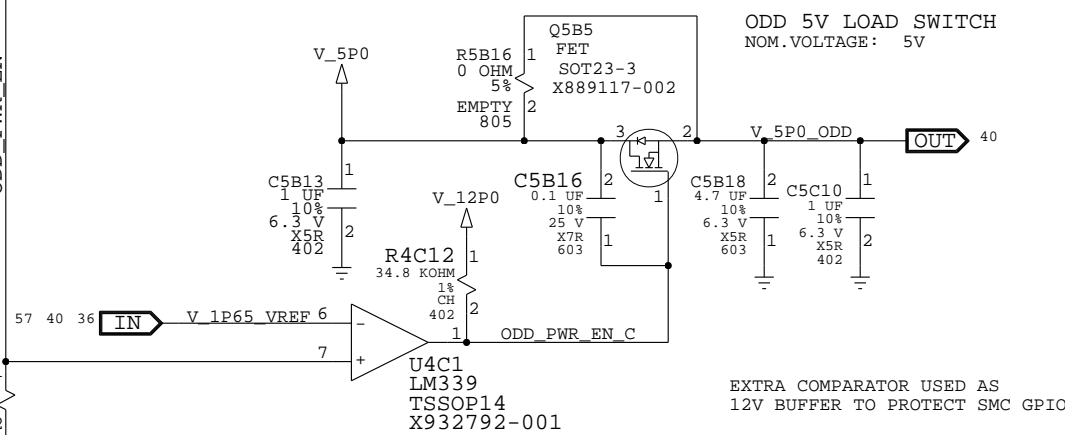
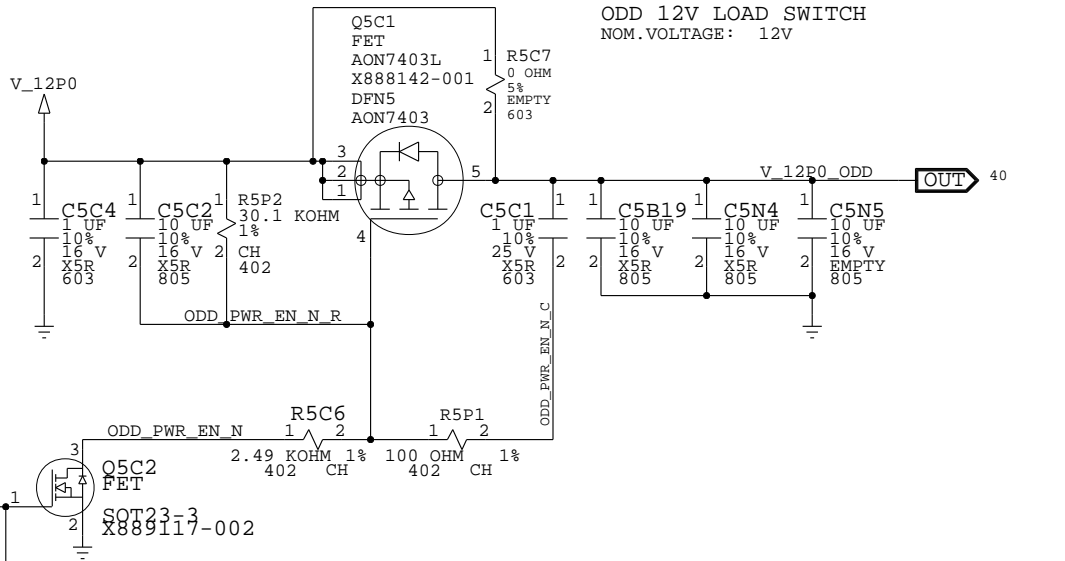
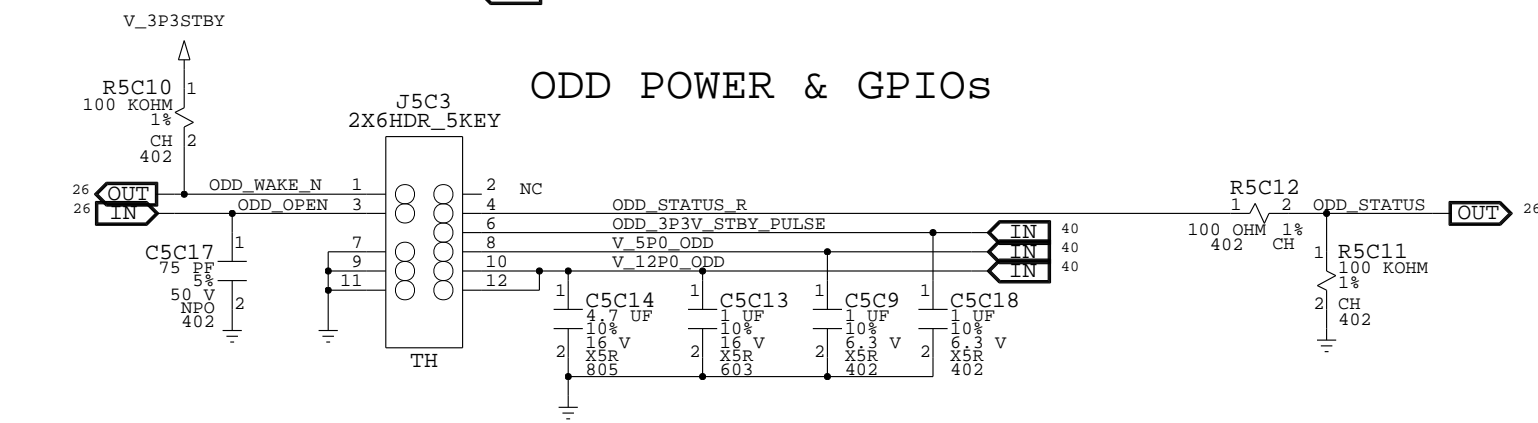
## HDD POWER



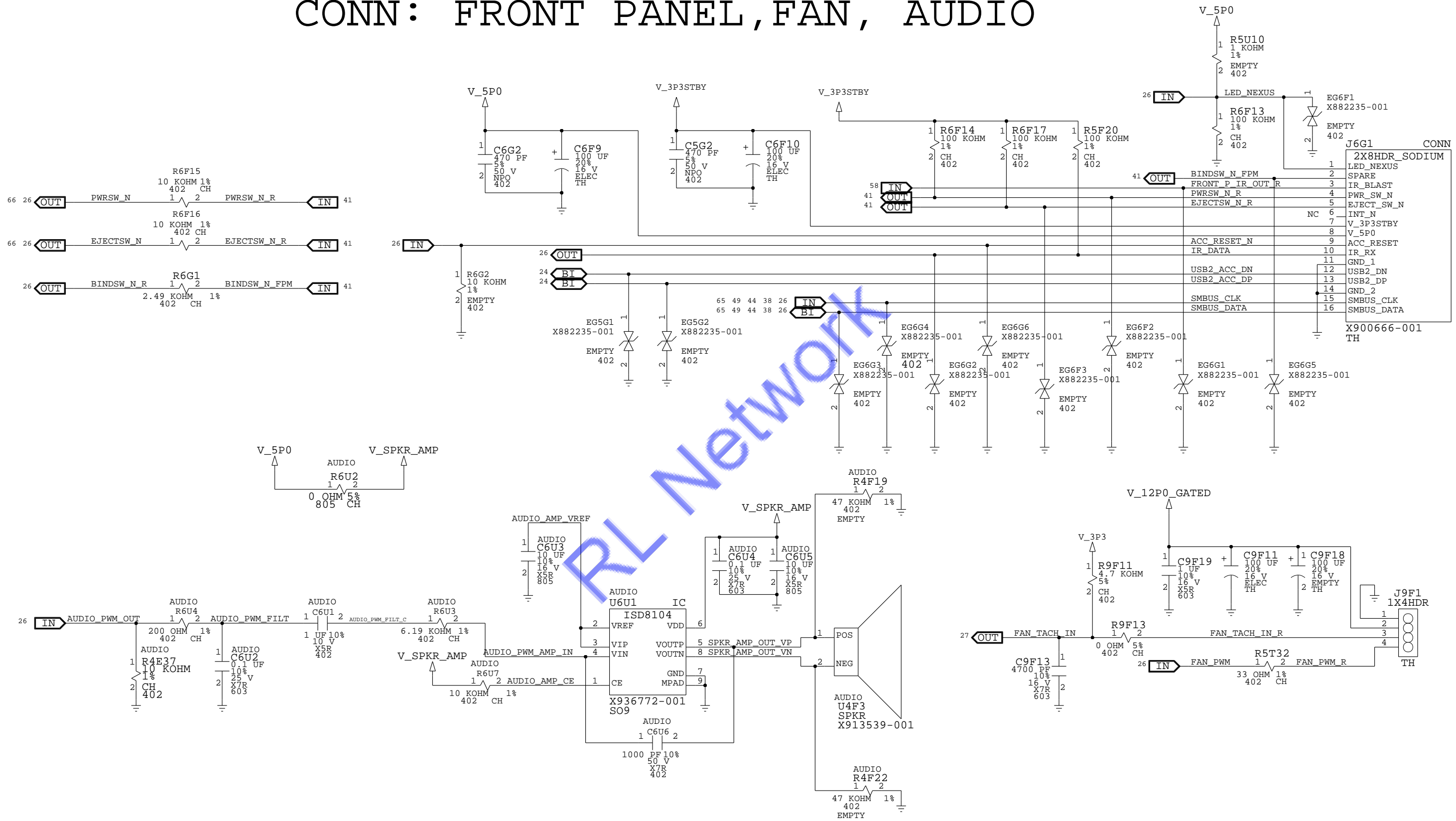
## V\_3P3STBY



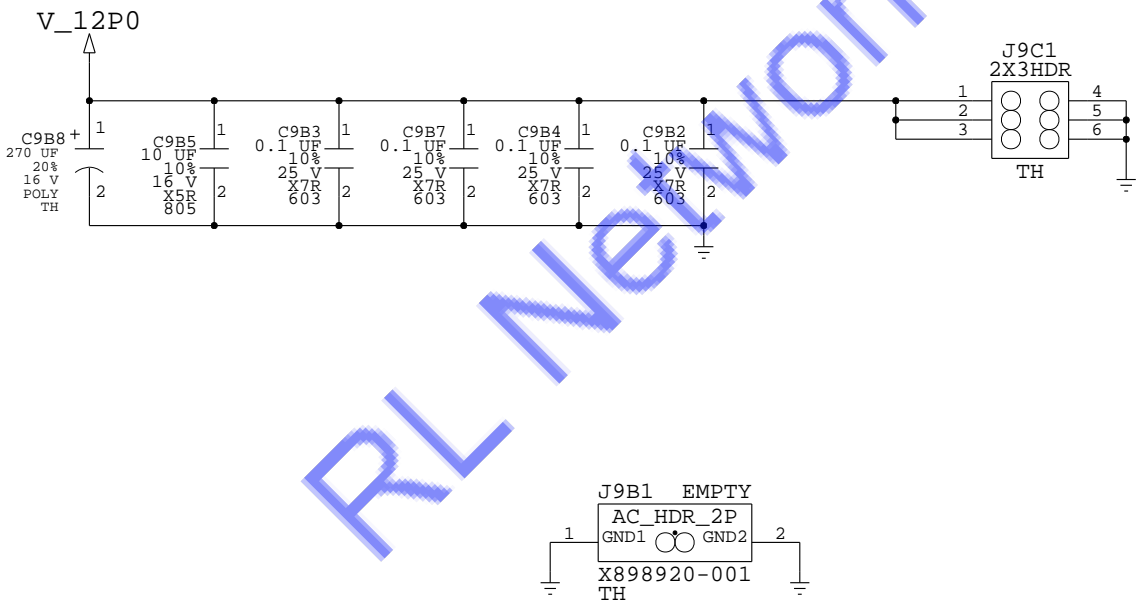
## ODD POWER & GPIOs



# CONN: FRONT PANEL, FAN, AUDIO

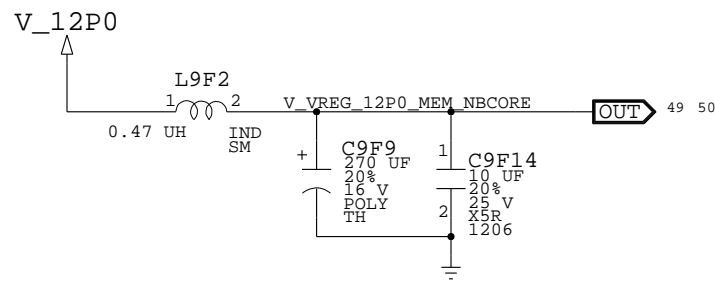


CONN: POWER

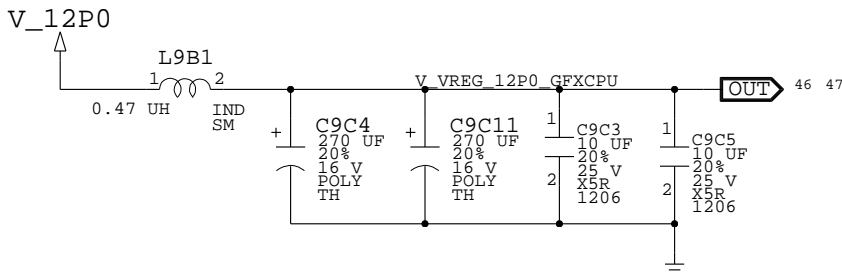


# VREGS: INPUT & OUTPUT FILTERS

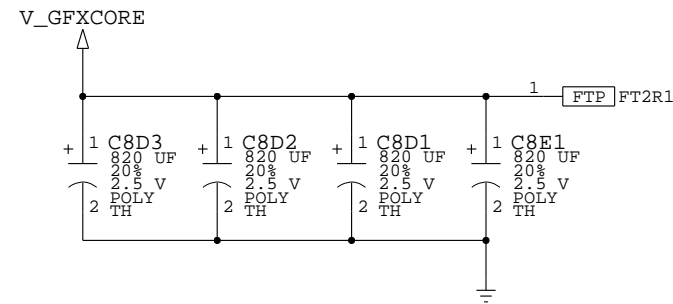
IO/NBCORE INPUT FILTER



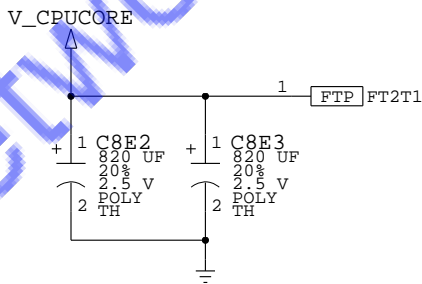
GFX/CPU INPUT FILTER



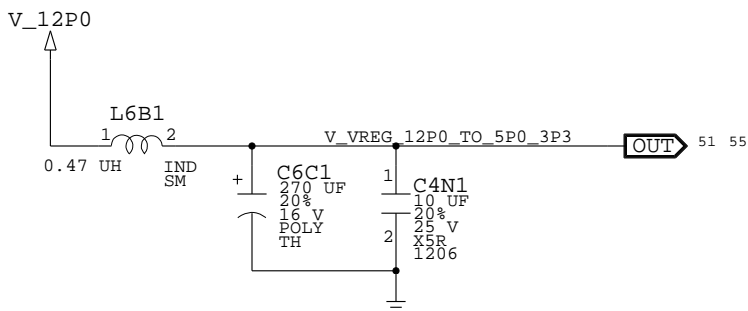
V\_GFXCORE OUTPUT FILTER



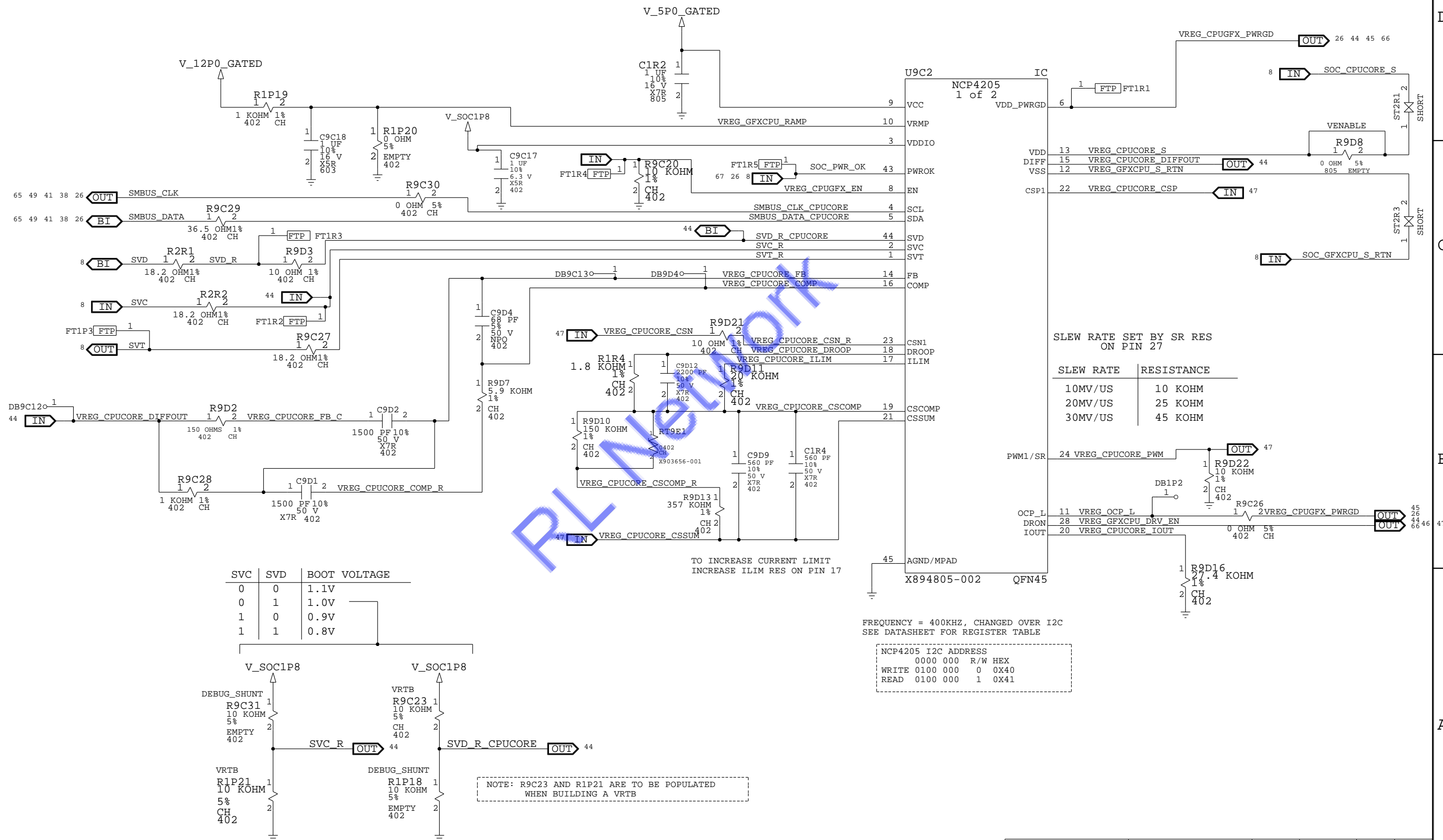
V\_CPUCORE OUTPUT FILTER



V\_5P0 AND V\_3P3 INPUT FILTER



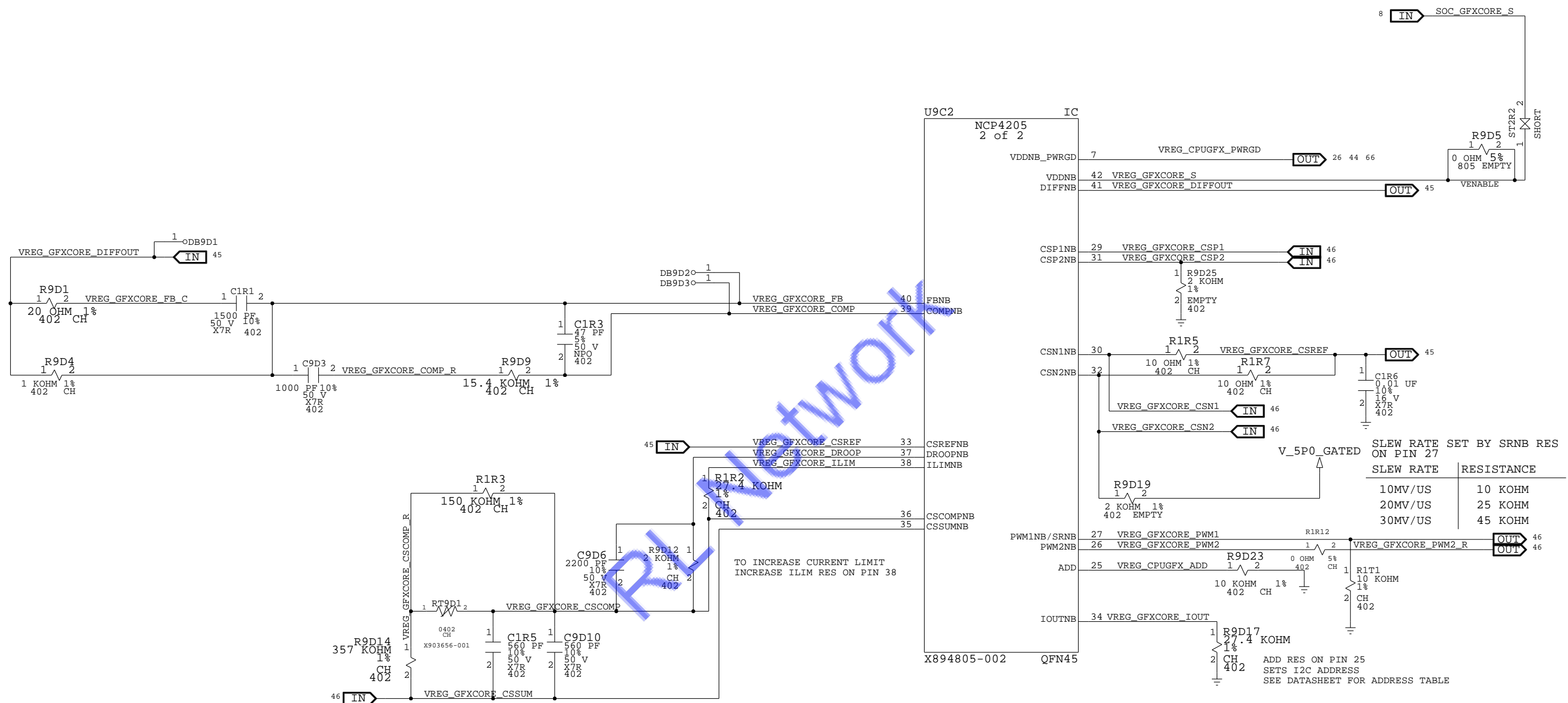
```
VREGS:  CPUCORE
```



MICROSOFT CONFIDENTIAL	PROJECT NAME Kingston	PAGE 44/72	CSA PAGE 44/72	FAB G	VER 1.01
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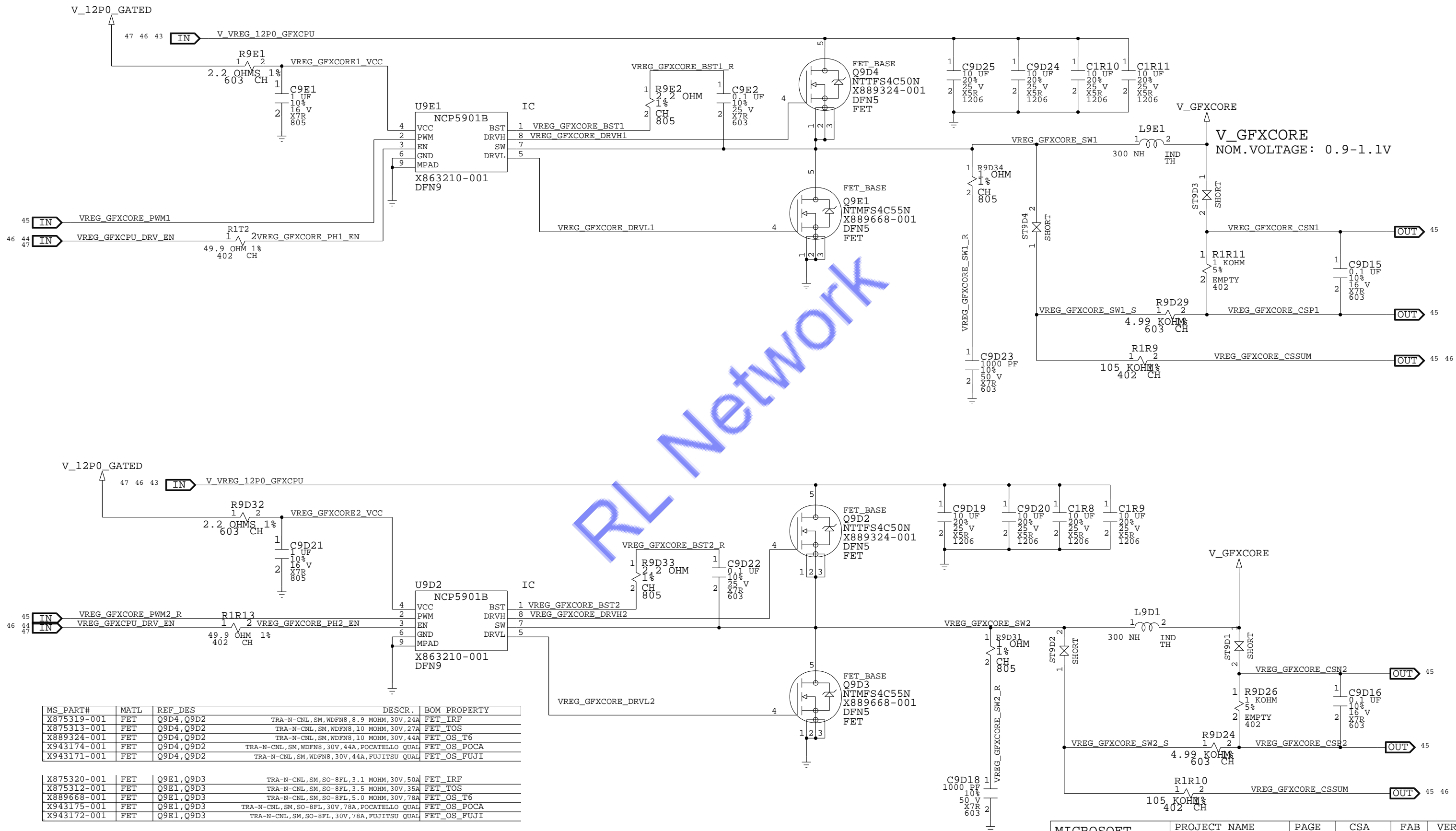


## VREGS: GFXCORE

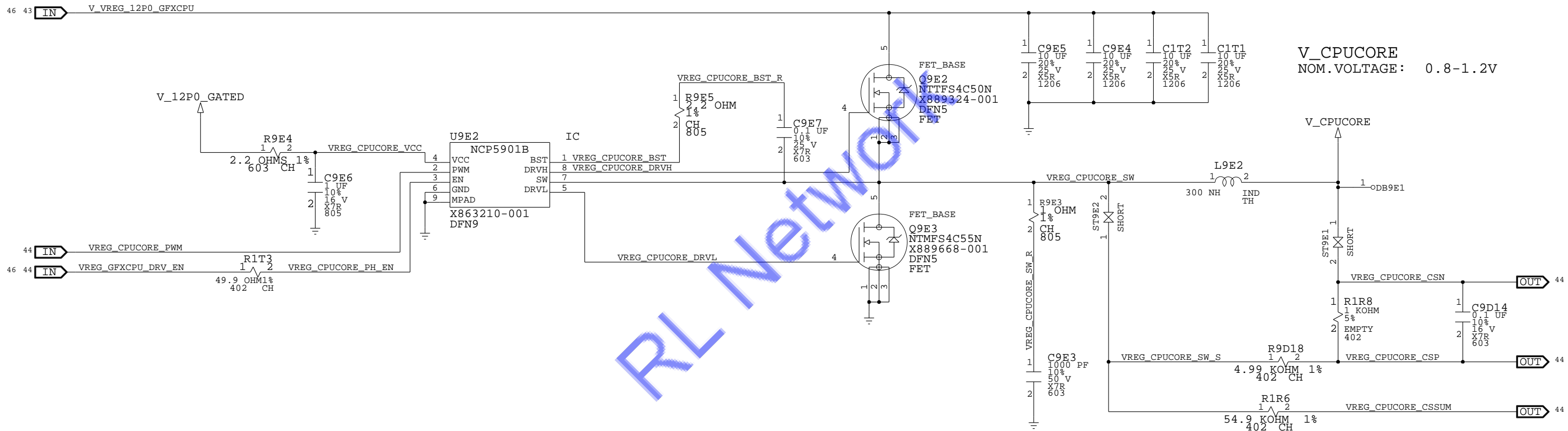


MICROSOFT CONFIDENTIAL	PROJECT NAME Kingston	PAGE 45/72	CSA PAGE 45/72	FAB G	VER 1.01
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# VREGS: GFXCORE OUTPUT PHASE 1 & 2



VREGS: CPUCORE OUTPUT PHASE

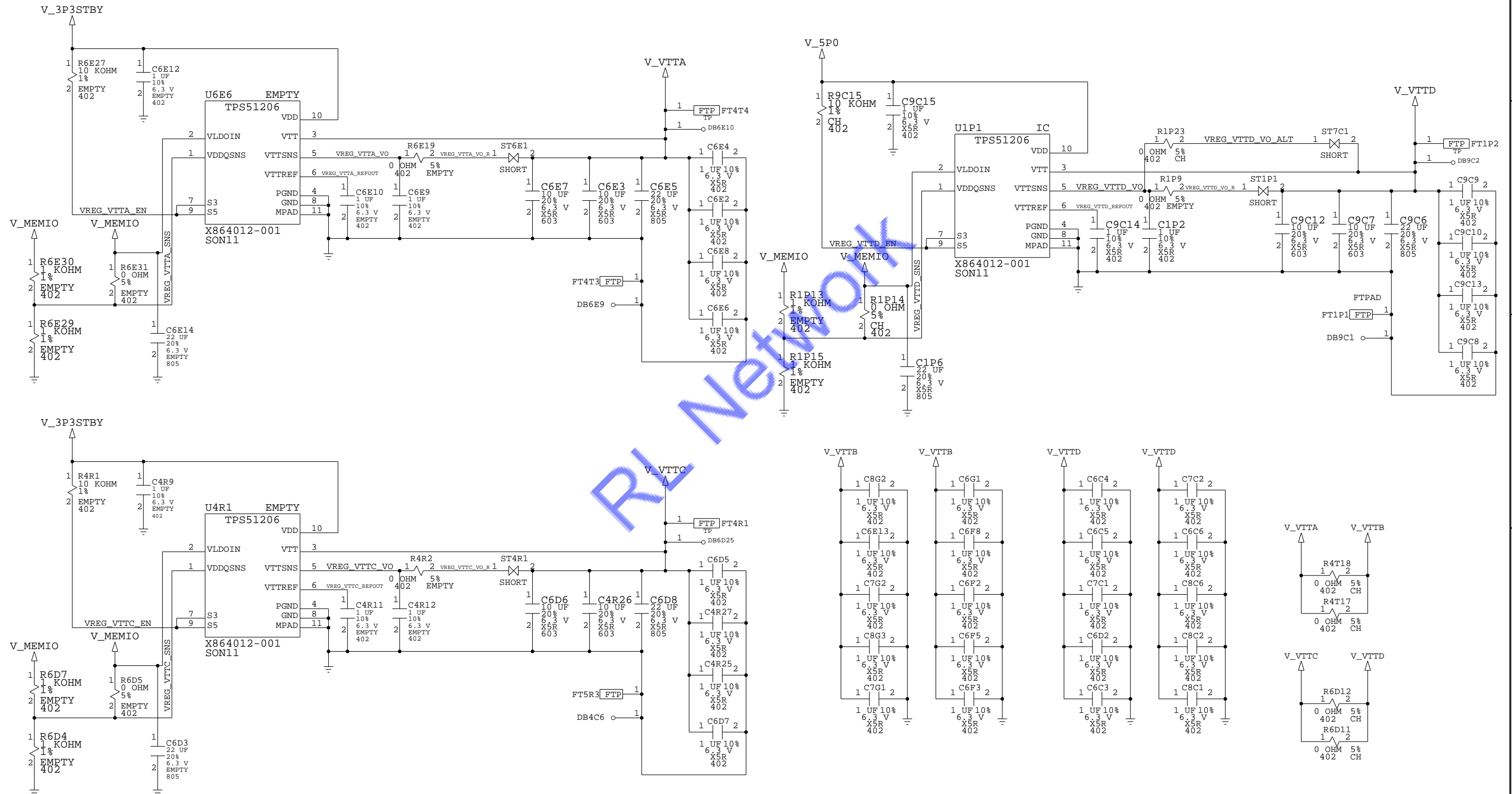


MS_PART#	MATL	REF_DES	DESCR.	BOM_PROPERTY
X875319-001	FET	Q9E2	TRA-N-CNL,SM,WDFN8,8.9 MOHM,30V,24A	FET_IRF
X875313-001	FET	Q9E2	TRA-N-CNL,SM,WDFN8,10 MOHM,30V,27A	FET_TOS
X889324-001	FET	Q9E2	TRA-N-CNL,SM,WDFN8,10 MOHM,30V,44A	FET_OS_T6
X943174-001	FET	Q9E2	TRA-N-CNL,SM,WDFN8,30V,44A,POCATELLO QUAL	FET_OS_POCA
X943171-001	FET	Q9E2	TRA-N-CNL,SM,WDFN8,30V,44A,FUJITSU QUAL	FET_OS_FUJI

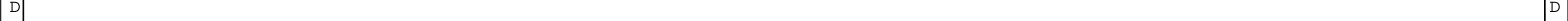
  

X875320-001	FET	Q9E3	TRA-N-CNL,SM,SO-8FL,3.1 MOHM,30V,50A	FET_IRF
X875312-001	FET	Q9E3	TRA-N-CNL,SM,SO-8FL,3.5 MOHM,30V,35A	FET_TOS
X889668-001	FET	Q9E3	TRA-N-CNL,SM,SO-8FL,5.0 MOHM,30V,78A	FET_OS_T6
X943175-001	FET	Q9E3	TRA-N-CNL,SM,SO-8FL,30V,78A,POCATELLO QUAL	FET_OS_POCA
X943172-001	FET	Q9E3	TRA-N-CNL,SM,SO-8FL,30V,78A,FUJITSU QUAL	FET_OS_FUJI

## VREGS: VTT TERMINATION



8	7	6	5	4	3	2	1
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B

FREQUENCY = 500KHz (SEE M3.130)	C5F10 4UF 1	VREG_NBCORE_OCP	4	TRIP	VO	5	VREG_NBCORE_VO	5	DB6E23
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B

A	X889668-001	FET	Q6F1	TRA-N-CNL,SM,SO-8FL,5.0 MOHM,30V,78A	FET OS T6
	X943175-001	FET	Q6F1	TRA-N-CNL,SM,SO-8FL,30V,78A,POCATELLO,78A	FET OS POCA



VREG: MEMIO

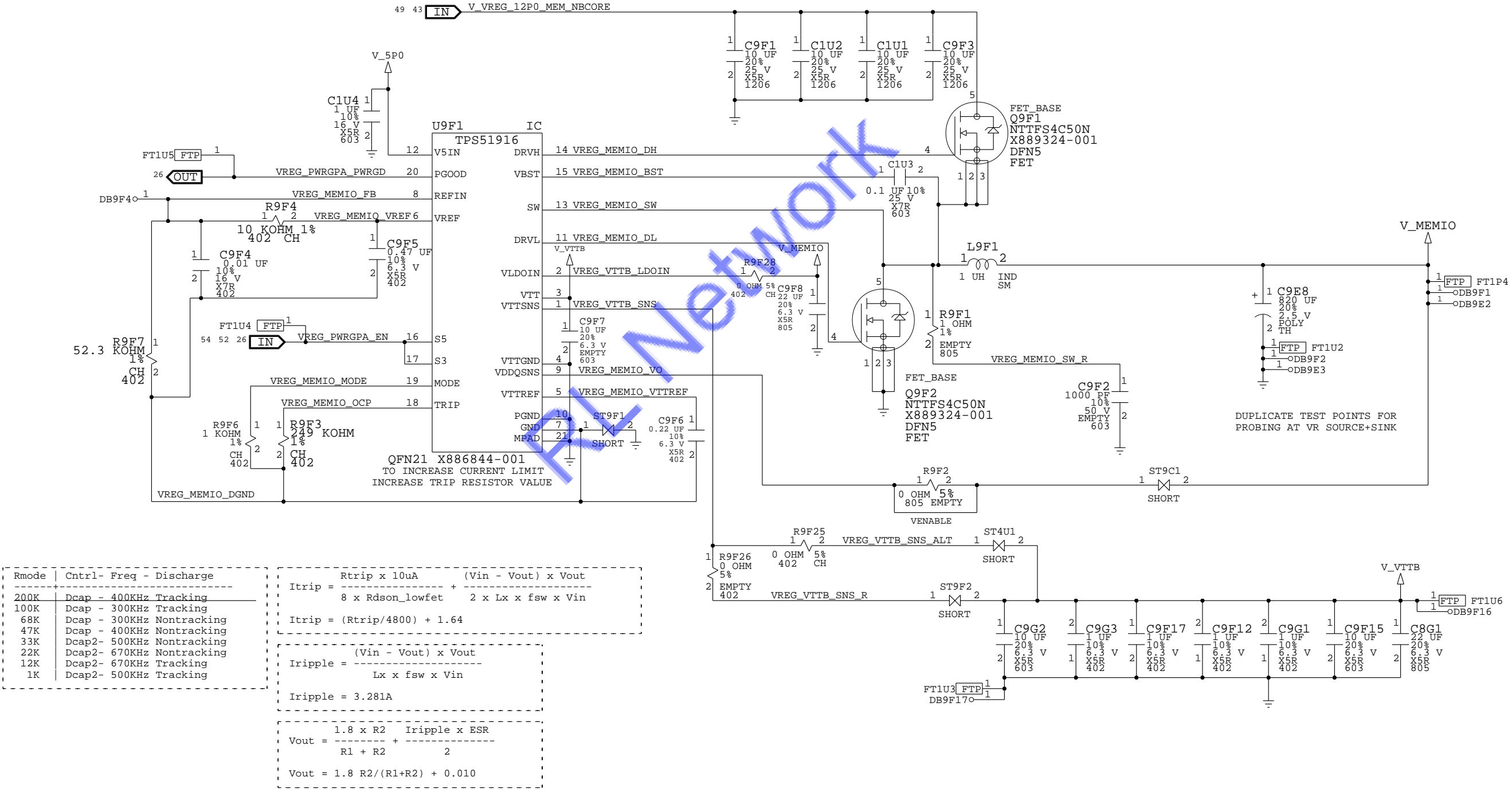
MS_PART#	MATL	REF_DES	DESCR.	BOM PROPERTY
X875319-001	FET	Q9F1	TRA-N-CNL,SM,WDFN8,8.9 MOHM,30 V,24 A	FET_IRF
X875313-001	FET	Q9F1	TRA-N-CNL,SM,WDFN8,10 MOHM,30 V,27 A	FET_TOS
X889324-001	FET	Q9F1	TRA-N-CNL,SM,WDFN8,10 MOHM,30 V,44 A	FET_OS_T6
X943174-001	FET	Q9F1	TRA-N-CNL,SM,WDFN8,30V,44A,POCATELLO QUAL	FET_OS_POCA
X943171-001	FET	Q9F1	TRA-N-CNL,SM,WDFN8,30V,44A,FUJITSU QUAL	FET_OS_FUJI

X875319-001	FET	Q9F2	TRA-N-CNL,SM,WDFN8,8.9 MOHM,30 V,24 A	FET_IRF
X875313-001	FET	Q9F2	TRA-N-CNL,SM,WDFN8,10 MOHM,30 V,27 A	FET_TOS
X889324-001	FET	Q9F2	TRA-N-CNL,SM,WDFN8,10 MOHM,30 V,44 A	FET_OS_T6
X943174-001	FET	Q9F2	TRA-N-CNL,SM,WDFN8,30V,44A,POCATELLO QUAL	FET_OS_POCA
X943171-001	FET	Q9F2	TRA-N-CNL,SM,WDFN8,30V,44A,FUJITSU QUAL	FET_OS_FUJI

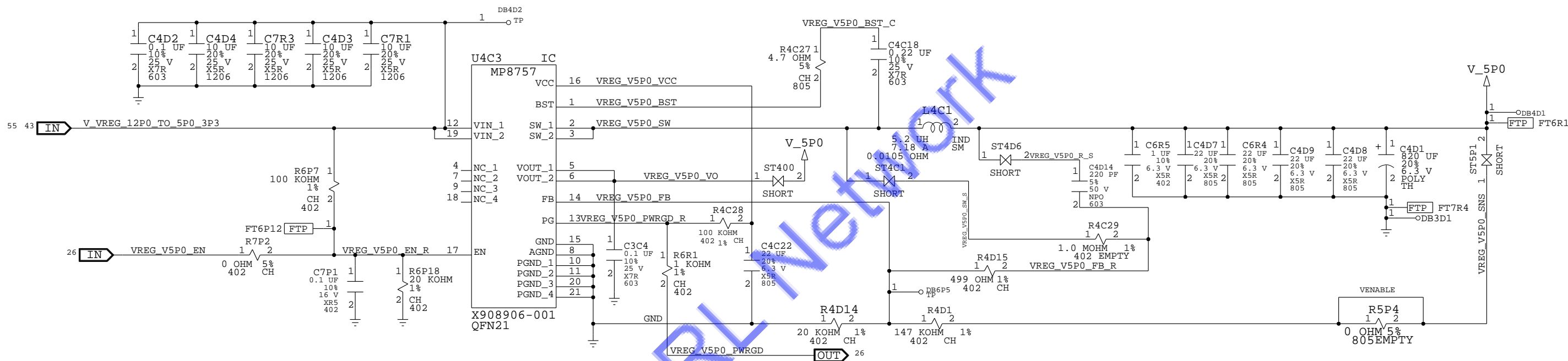
Q9F2 MATCHES Q9F1

V\_MEMIO  
NOM. VOLTAGE: 1.50

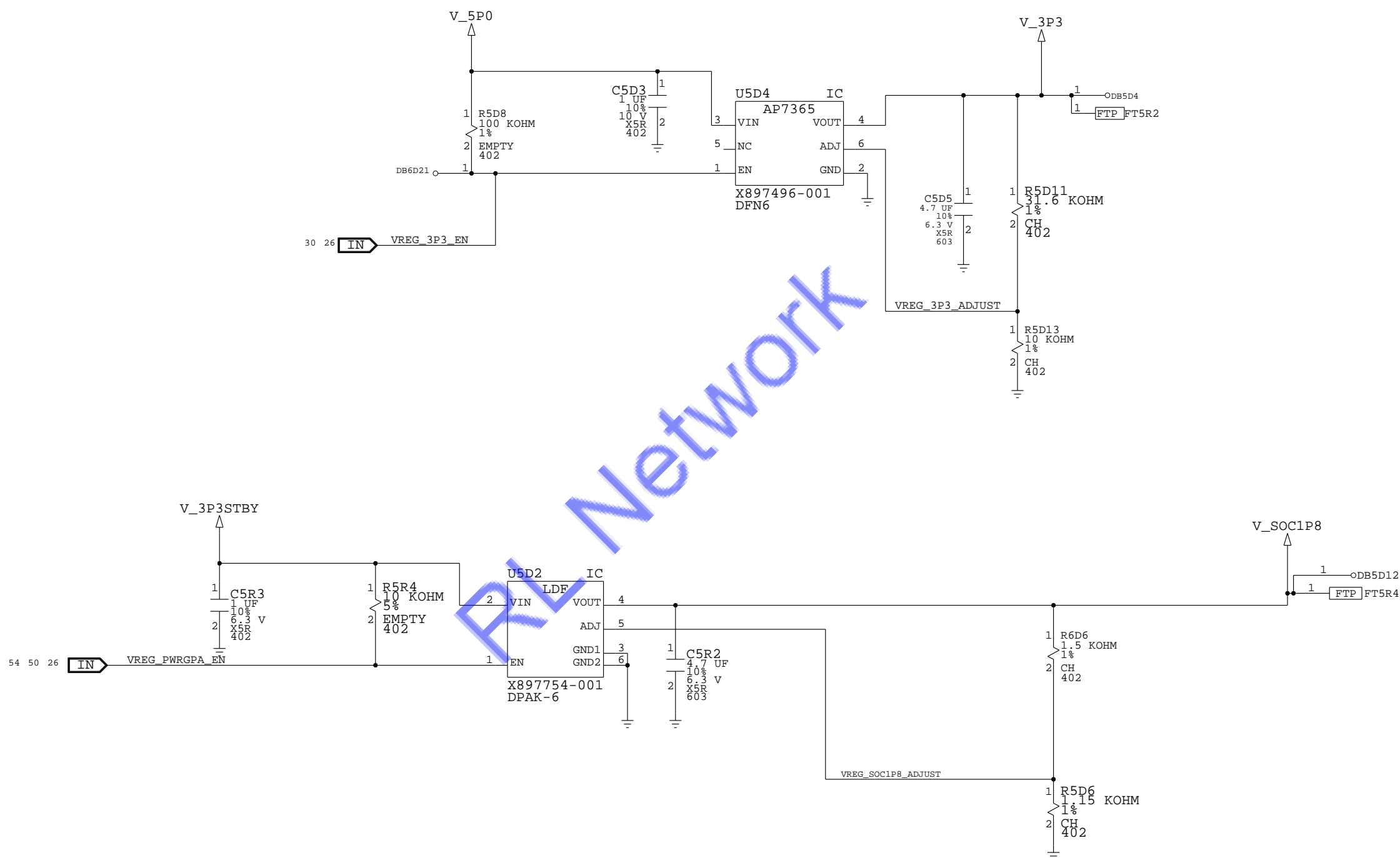


# VREGS: V5P0

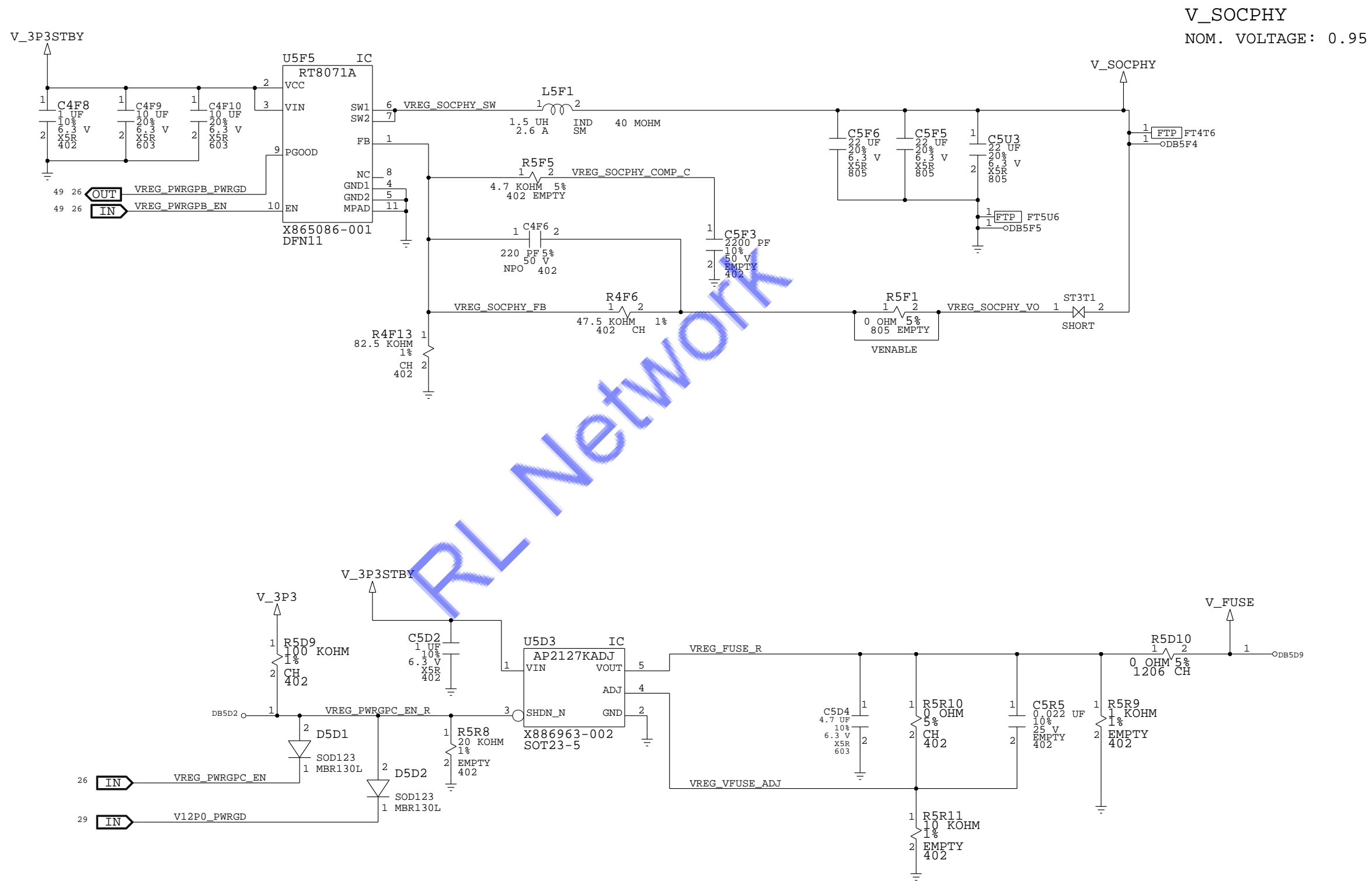
V\_5P0  
NOM. VOLTAGE: 5.09



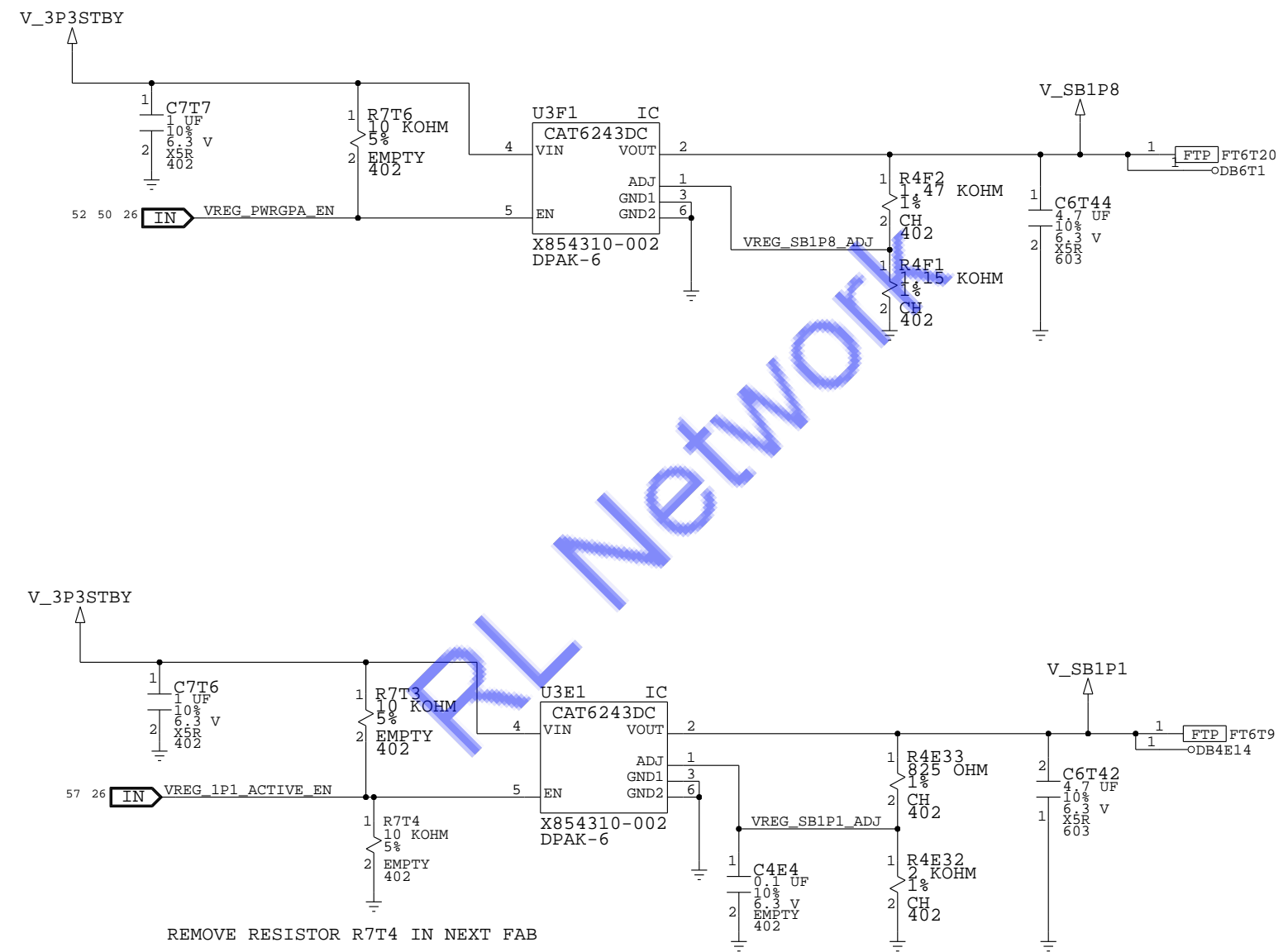
VREGS: V3P3, VSOC1P8



# VREGS: VSOCPHY/VFUSE



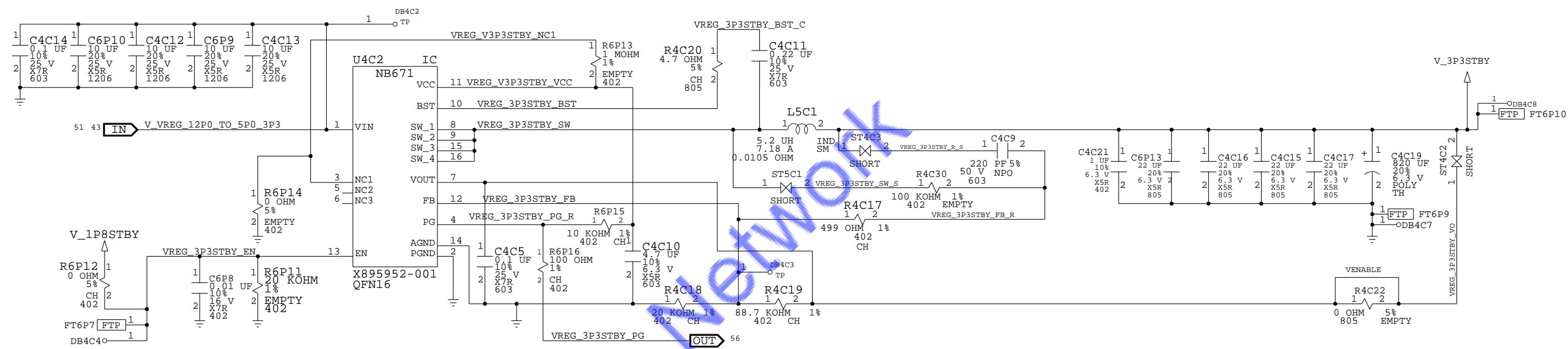
VREGS: V\_SB1P8, V\_SB1P1



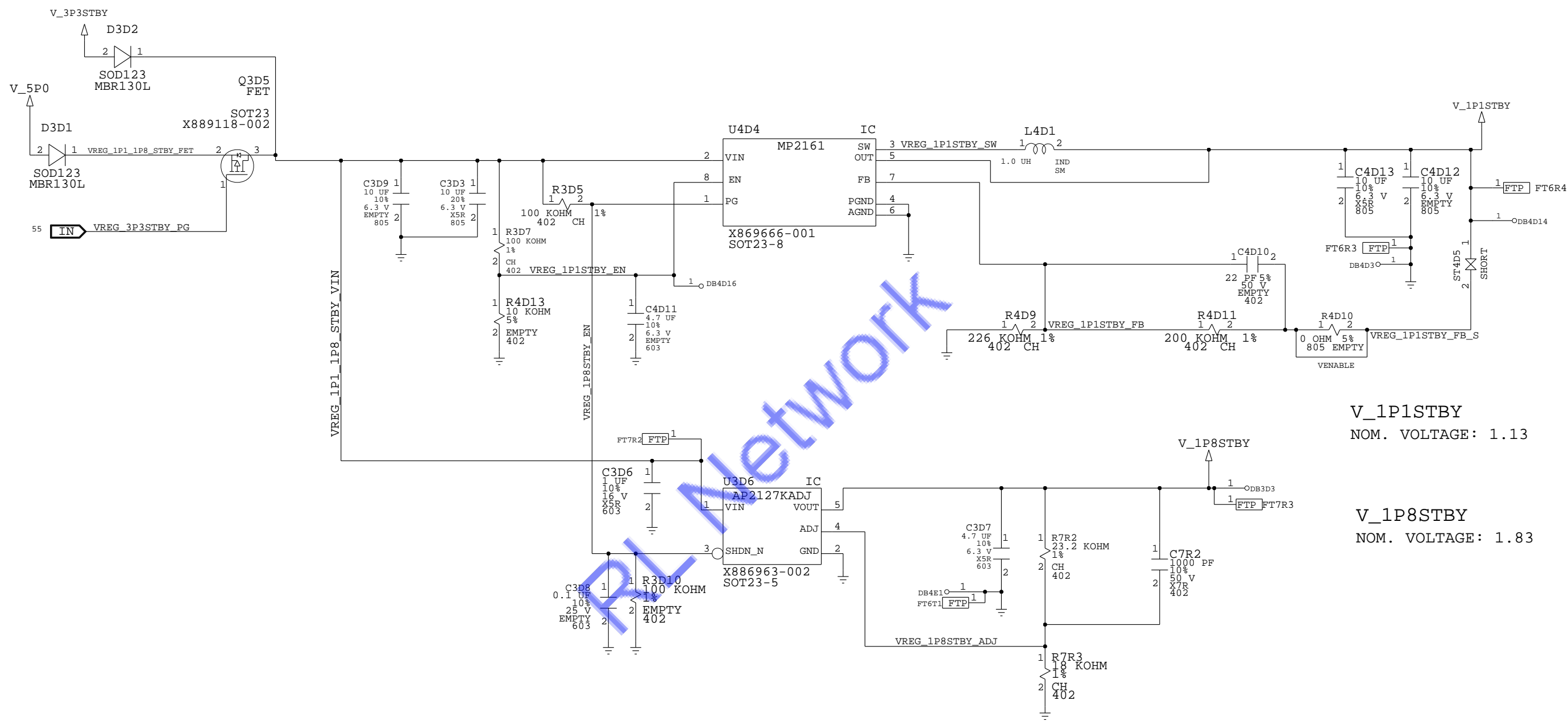


VREGS: V3P3 STANDBY

V\_3P3STBY  
NOM. VOLTAGE: 3.31



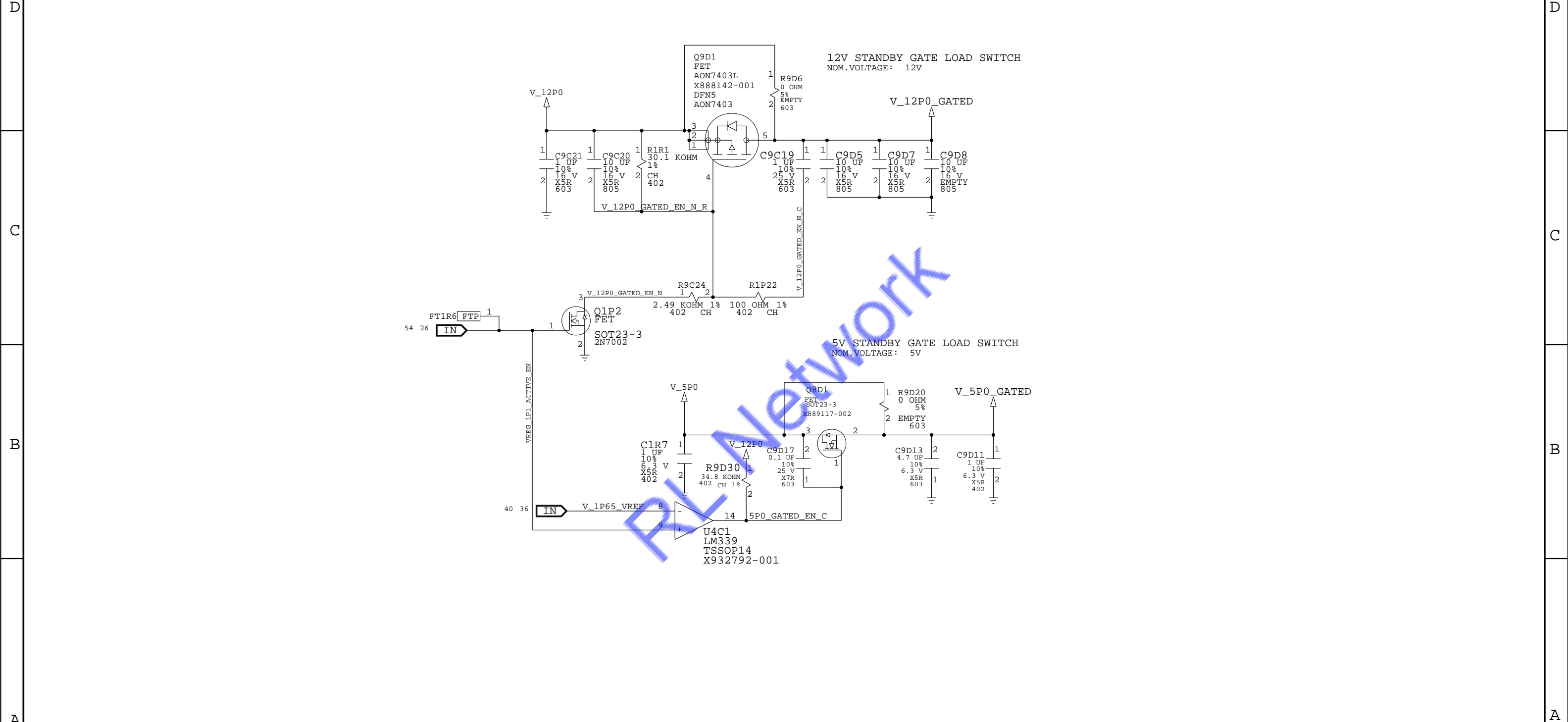
VREGS: V1P1 STANDBY, V1P8 STANDBY



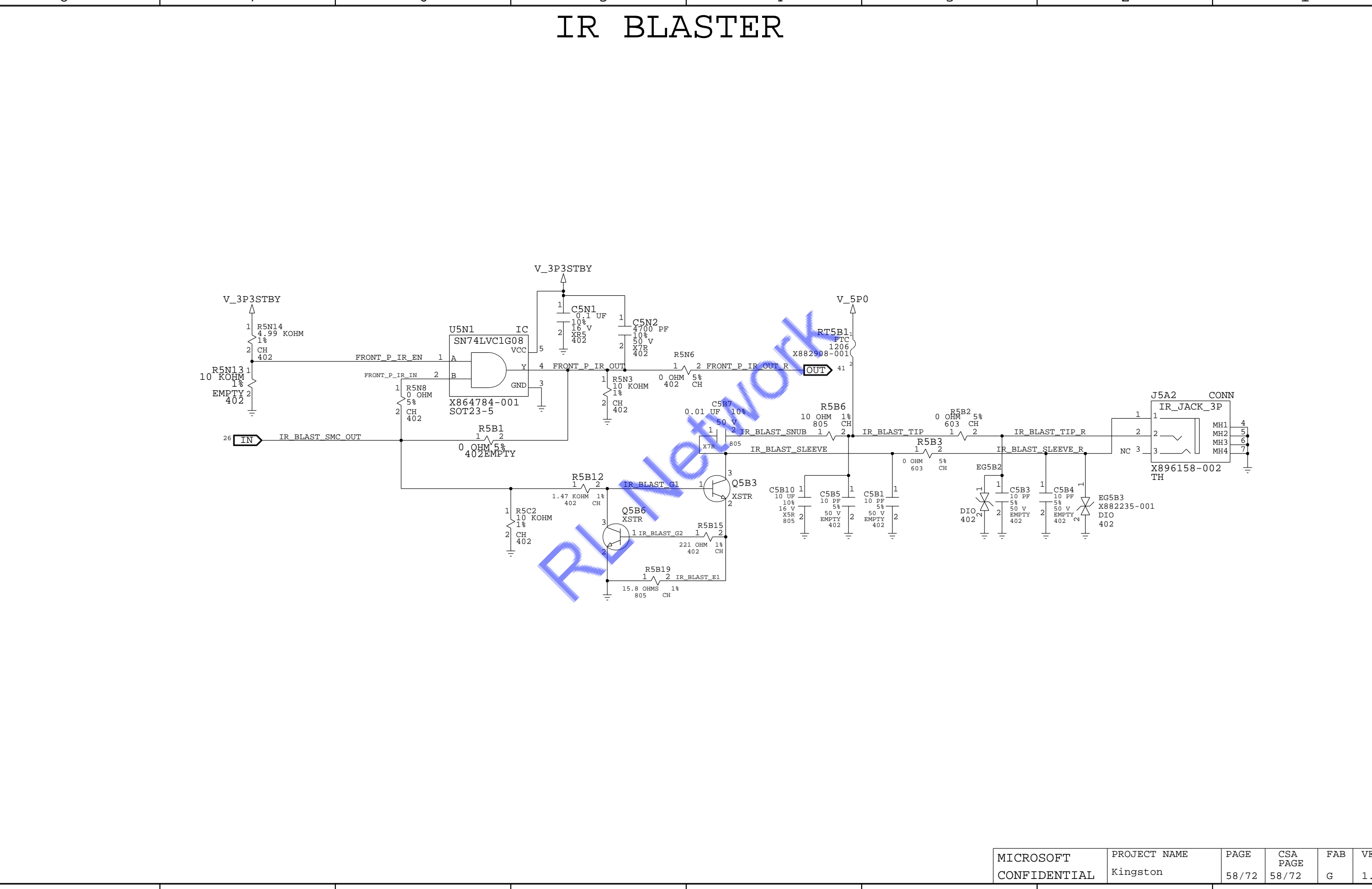
V\_1P1STBY  
NOM. VOLTAGE: 1.13

V\_1P8STBY  
NOM. VOLTAGE: 1.83

8	7	6	5	4	3	2	1
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8	7	6	5	4	3	2	1
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I2C

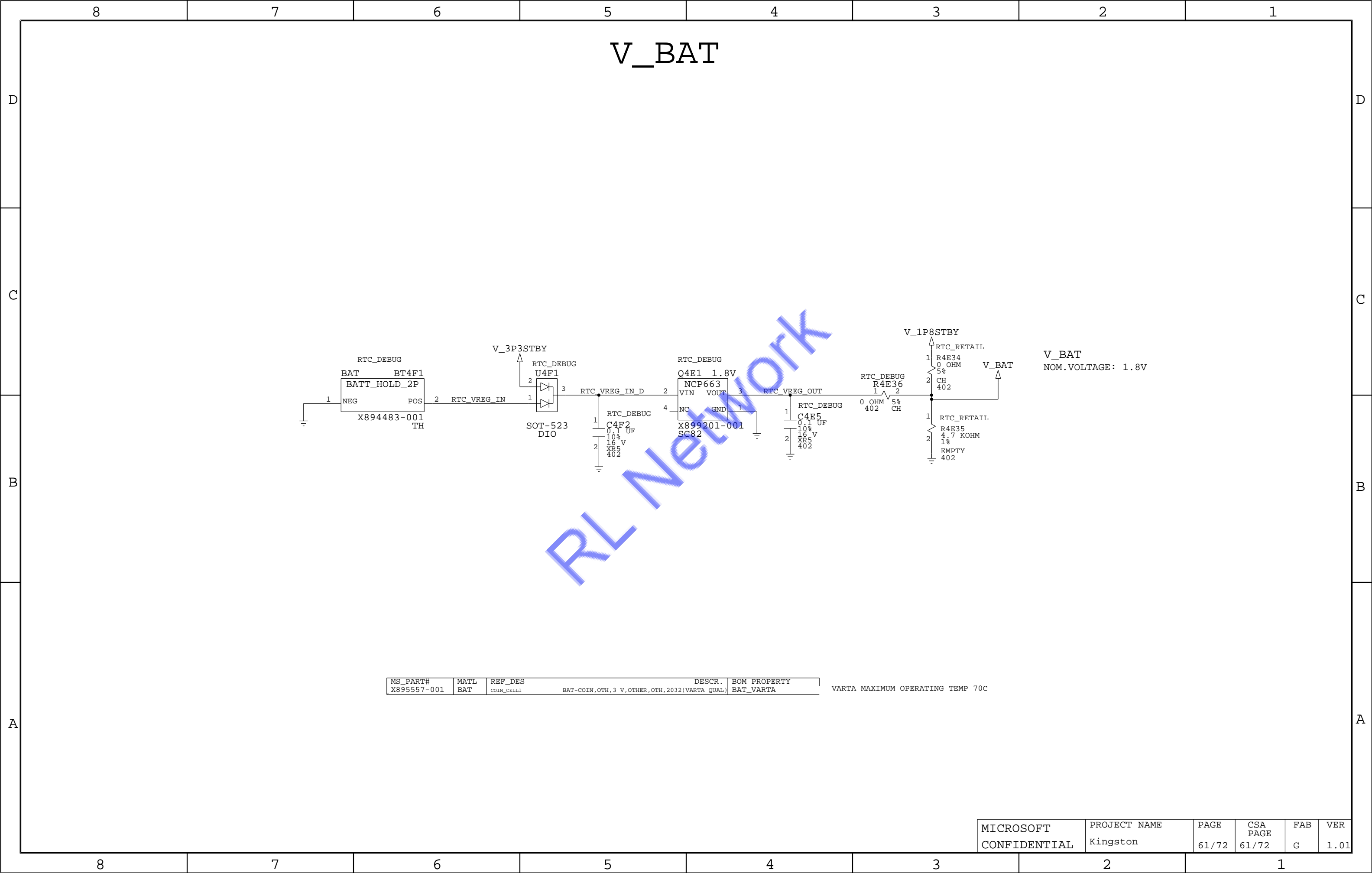
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MICROSOFT CONFIDENTIAL	PROJECT NAME Kingston	PAGE 59/72	CSA PAGE 59/72	FAB G	VER 1.01
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8		7		6		5		4		3		2		1	
MARGIN: SOCPHY ,SOC1P8 ,MEMIO ,NBCORE															
D														D	
C														C	
B														B	
A														A	
8		7		6		5		4		3		2		1	



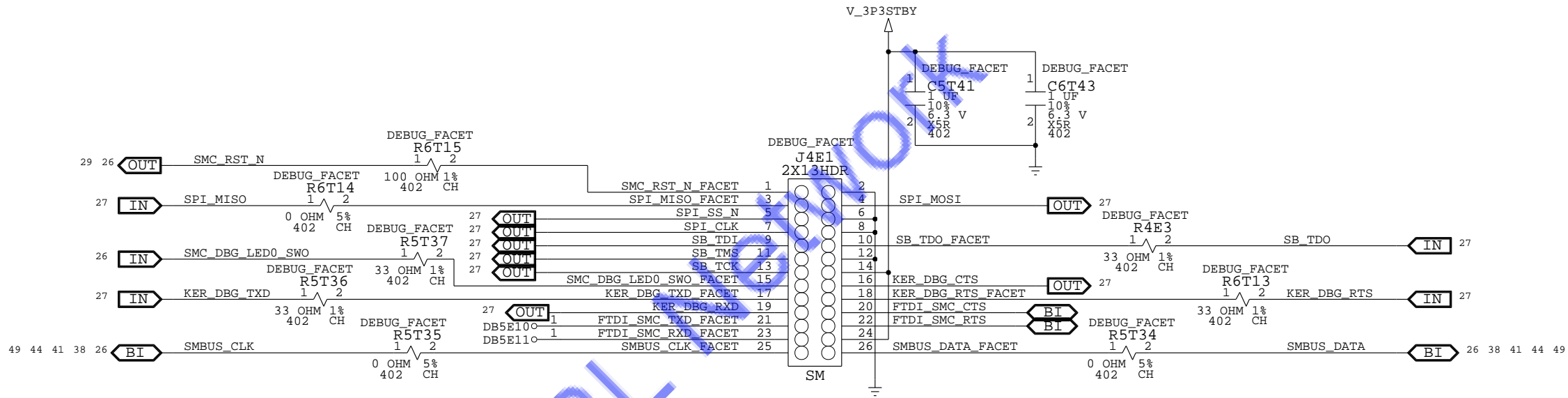


8		7		6		5		4		3		2		1			
MONITOR : NBCORE , MEMIO																	
D															D		
C															C		
B															B		
A															A		
8		7		6		5		4		3		2		1			
												MICROSOFT CONFIDENTIAL	PROJECT NAME Kingston	PAGE 62/72	CSA PAGE 62/72	FAB G	VER 1.01

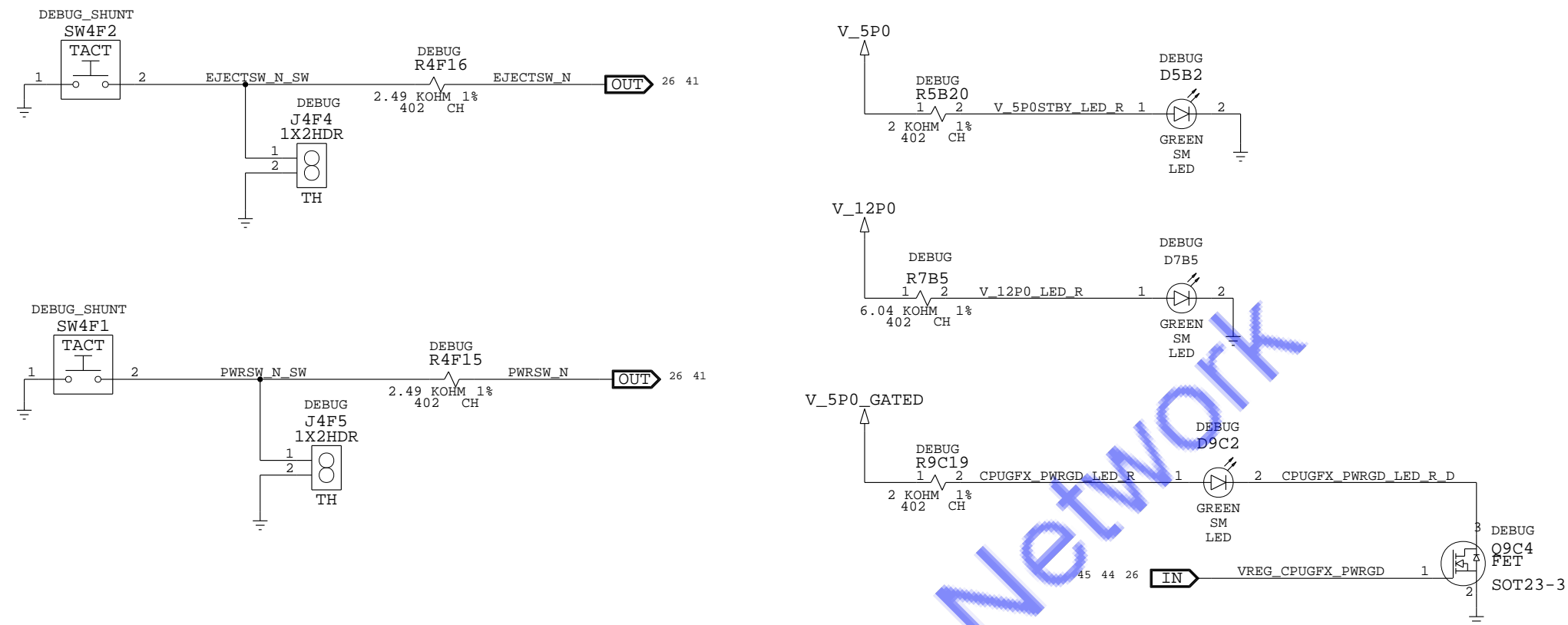
8		7		6		5		4		3		2		1	
MONITOR: VSOC1P8,VSOCPHY															
D														D	
C														C	
B														B	
A														A	
8		7		6		5		4		3		2		1	

8		7		6		5		4		3		2		1	
MONITOR: V12P0															
D														D	
C														C	
B														B	
A														A	
8		7		6		5		4		3		2		1	

CONN: FACET BOARD

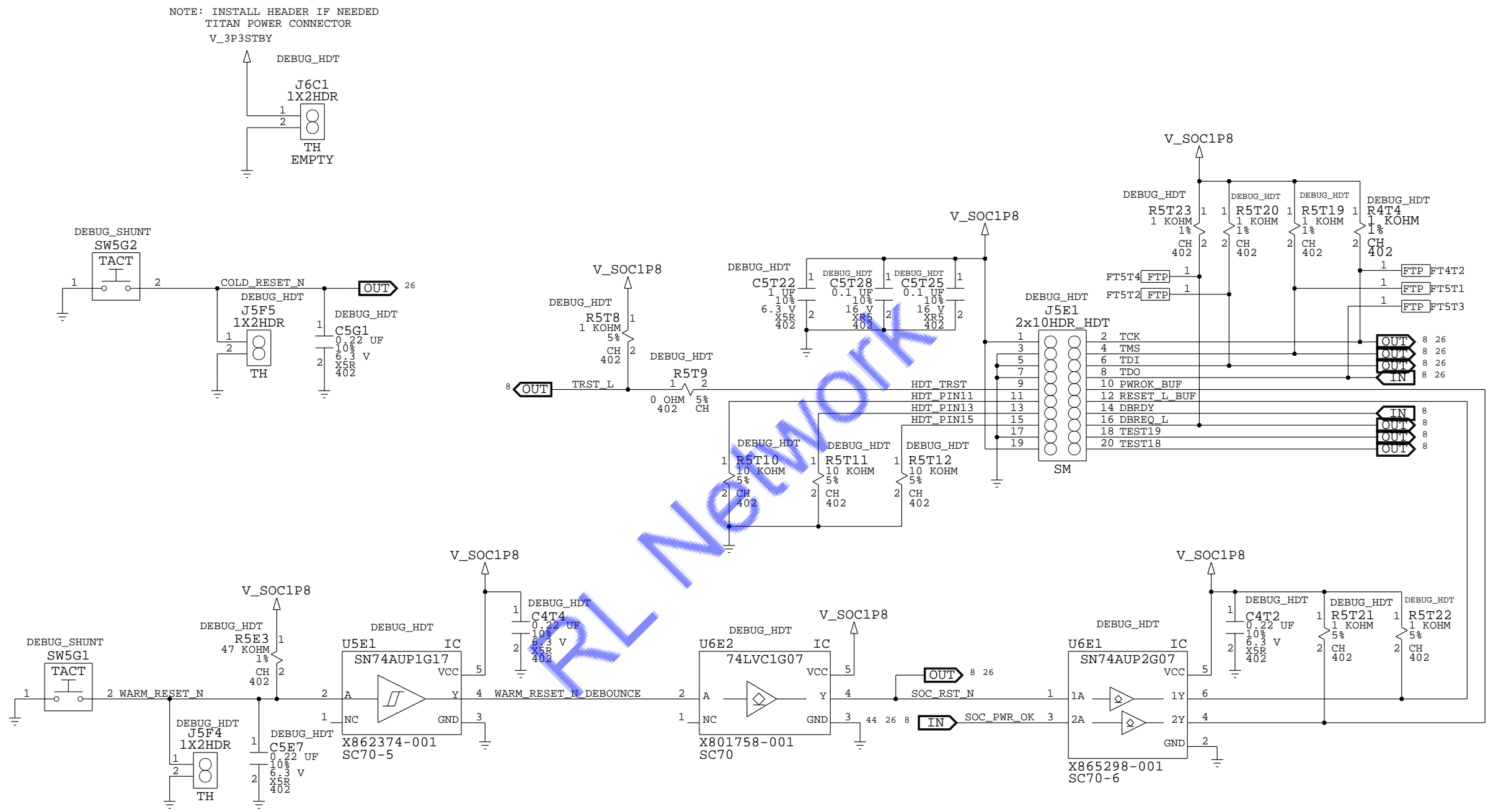


CONN: SWITCHES

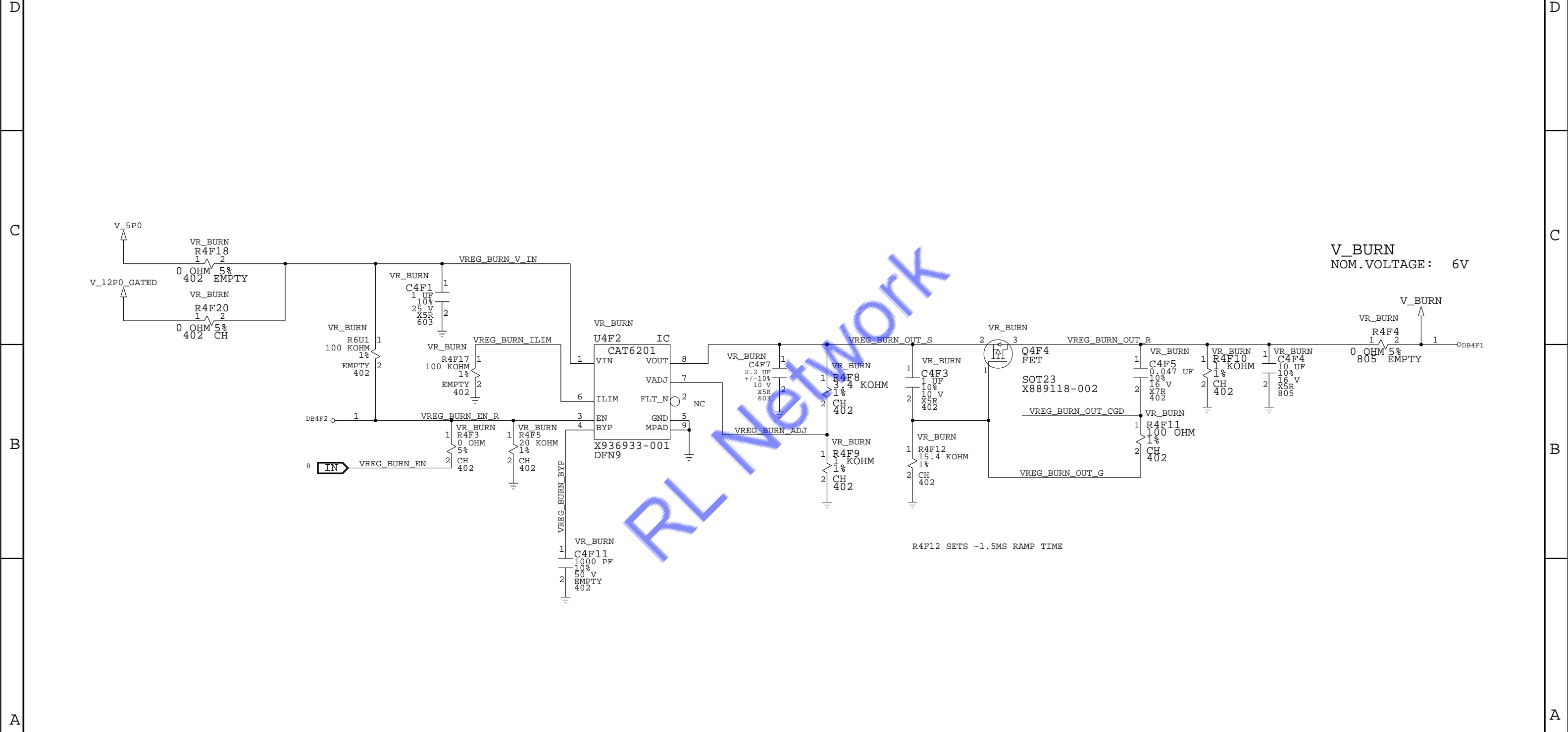




CONN: HDT



8	7	6	5	4	3	2	1
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R4F12 SETS ~1.5MS RAMP TIME

8	7	6	5	4	3	2	1
---	---	---	---	---	---	---	---



## DEBUG: CONNECTORS

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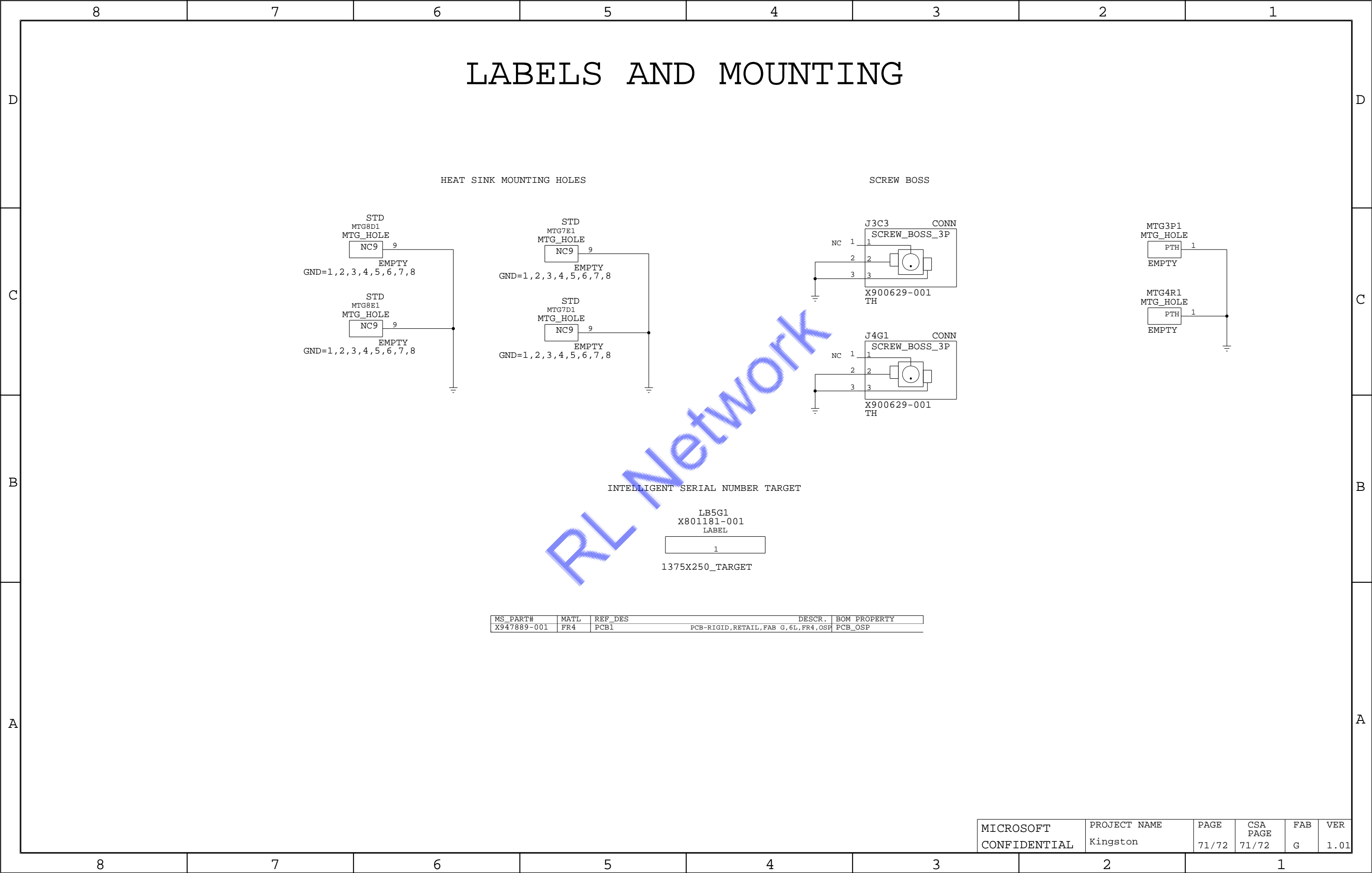
MICROSOFT  
CONFIDENTIAL

PROJECT NAME
Kingston

PAGE  
70/72

CSA PAGE 70/72	
----------------------	--

VER
1.01



8		7		6		5		4		3		2		1							
D	BOM DEFINITIONS														D						
	BOM		DEFINTION																		
	AUX		HDMI STUFFING OPTION. NEVER USED IN PRODUCTION. REWORK PURPOSES ONLY																		
	COMMON		ALL COMPONENTS WITH NO BOM PROPERTY																		
C	DDC		HDMI STUFFING OPTION. ALWAYS USED IN PRODUCTION													C					
	DDR_BASE		DUMMY PLACE HOLDER FOR DDR3 DEVICES. NEVER USE THIS IN THE RECIPE FILE. SELECT ONE OF THESE 3 INSTEAD: DDR_HYNIX, DDR_MICRON, DDR_SAMSUNG																		
	DDR_HYNIX		HYNIX DDR3																		
	DDR_MICRON		MICRON DDR3																		
B	DDR_SAMSUNG		SAMSUNG DDR3													B					
	DEBUG		COMPONENTS REQUIRED FOR BRING UP & DEBUG																		
	DEBUG_HDT		HDT-RELATED DEBUG COMPONENTS																		
	DEBUG_HDMI		DEBUG HDMI CONNECTOR USED 8L DEBUG BOARDS																		
A	DEBUG_SHUNT		COMPONENTS WHICH ARE ON DEBUG BOARDS, BUT ARE REMOVED/SHORTED ON RETAIL													A					
	EMMC_BASE		DUMMY PLACE HOLDER FOR EMMC DEVICE & RESISTORS. NEVER USE THIS IN THE RECIPE FILE. SELECT ONE OF THESE INSTEAD: EMMC_HYNIX_20NM, EMMC_HYNIX_5P0, EMMC_HYNIX_1XNM, EMMC_SAMSUNG AND EMMC_TOSHIBA																		
	EMMC_HYNIX_5P0		HYNIX EMMC V5.0 EMMC DEVICE																		
	FET_BASE		DUMMY PLACE HOLDER FOR HIGH AND LOW FETS. NEVER USE THIS IN THE RECIPE FILE. SELECT ONE OF THESE INSTEAD: FET_AOS, FET_OS_T6, FET_STM, OR FET_TOS																		
B	FET_IRF		INTERNATIONAL RECTIFIER FETS USED FOR VOLTAGE REGUALTORS													B					
	FET_OS_T6		ON-SEMI T6 FETS USED FOR VOLTAGE REGULATORS																		
	FET_STM		STMICROELECTRONICS FETS USED FOR VOLTAGE REGULATORS																		
	FET_TOS		TOSHIBA FETS USED FOR VOLTAGE REGULATORS																		
A	GARFIELD		CONTAINS GARFIELD (SOC) RELATED PASSIVE/ACTIVE COMPONENTS													A					
	KIC_BASE		DUMMY PLACE HOLDER FOR KIC. NEVER USE THIS IN THE RECIPE FILE. USE ONE OF THESE INSTEAD: KIC_DEV OR KIC_RETAIL																		
	KIC_DEV		DEBUG VERSION OF KRAKEN																		
	KIC_RETAIL		RETAIL VERSION OF KRAKEN																		
B	MEM_FIXED		SETS V_MEMIO TO A FIXED VOLTAGE (NON-MARGINED). MUST BE USED IN CONJUNCTION WITH NOT MEM_MM													B					
	MEM_MM		ALLOWS V_MEMIO TO BE MARGINED FOR M&M BOARDS. MUST BE USED IN CONJUNCTION WITH NOT MEM_FIXED																		
	PANTHER		CONTAINS PANTHER (SOC) RELATED PASSIVE/ACTIVE COMPONENTS																		
	PANTHER_SOC		PANTHER SYSTEM-ON-CHIP (SOC)																		
A	PANTHER_SOC_LP		PANTHER SYSTEM-ON-CHIP (SOC) LOW POWER VERSION													A					
	PCB_GI		FAB TYPE: GOLD																		
	PCB_OSP		FAB TYPE: ORGANIC SOLDERABILITY PRESERVATIVE																		
	RTC_RETAIL		RTC CIRCUIT IMPLEMENTATION FOR RETAIL BOARDS																		
A	RTC_DEBUG		RTC CIRCUIT IMPLEMENTATION FOR DEBUG BOARDS													A					
	SOC_BASE		DUMMY PLACE HOLDER FOR SOC																		
	VR_FIXED		SET ALL VRS TO FIXED VOLTAGES (NON-MARGINED). EXCLUDES V_MEMIO. MUST BE USED IN CONJUNCTION WITH NOT VR_MM																		
	VR_MM		ALLOWS MOST VRS TO BE MARGINED FOR M&M BOARDS. EXCLUDES V_MEMIO. MUST BE USED IN CONJUNCTION WITH NOT VR_FIXED																		
A	VRTB		BOOT STRAPPING RESISTOR ONLY TO BE POPULATED WHEN BUILDING VOLTAGE REGULATOR TEST BOARD WHICH CONTAINS NO SOC													A					
	WW		CAPACITORS WHICH NEED TO BE NO-STUFFED WHEN AI CPU/GPU SOCKET IS INSTALLED																		
8		7		6		5		4		3		2		1							
														MICROSOFT CONFIDENTIAL		PROJECT NAME Kingston		PAGE 72/72	CSA PAGE 72/72	FAB G	VER 1.01